

PCB Number: 10128 -1A

Project Code: 91.3FC01.001 / 91.3FM01.001

Project Name: PIH61L/eZappa-AIO

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BOM PARAMETER

I: Intel GLAN

K: Realtek GLAN

~~A: LAN support ASF~~

N: LAN don't support ASF

G: GPU SKU

V: Veriton (TPM and COM)

S: Scalar SKU

U: UMA

V_GPU:K,G,V,S

V_UMA:K,V,S,U

E_GPU:K,G,S,N

E_UMA:K,S,U,N

~~NOTE: (mount R80 71.08111 J03,R1125 63.10334 1DL)~~

PCB BOARD SIZE
214mmX 218mm
6 Layer

Internal Slot/Header
Front/Rear IO
Chipset

VRM 12
(3 Phase 65W)

INTEL
Sandy Bridge
SOCKET FCLGA LGA1155
(65W)
0.9144mmX0.9144mm

Channel A
64 bit
1066/1333MHZ

DDR3 SO-DIMM

Channel B
64 bit
1066/1333MHZ

DDR3 SO-DIMM

PCI-E x16 BUS

100MHz

PECI 3.0

PECI

14.318MHz

33MHz

24MHz; or 48MHz

96MHz

100 MHz

120 MHz

PCH
CLOCK
Buffer

25M

Page 20

LVDS

SCALAR
RTD2281W

DVI

INTEL PCH
Sugar Bay

SATA2.0 BUS

SATA *1
Slim ODD

SATA2.0 BUS

SATA *1
3.5" HDD

D-SUB PORT

RGB

PCIE Gen1 Interface

MINI PCI-E
WLAN

PCIE Gen1 Interface

LAN
82579LM

RJ45

PCIE Gen1 Interface

LAN
RTL8111E

120MHz

100MHz

96MHz

48MHz

33MHz

14.318MHz

32.768KHz

32.7K

USB2.0X2 SIDE

USB 2.0 *10

480Mb/s

USB 2.0 x4 REAR

WEBCAM/TOUCH PANEL/BT

CARD READER RTS5139
SD BOOT

SPI Flash ROM

32Mb

SPI BUS

REAR
Speaker

HDA CODEC
ALC269Q VB5

High Definition Audio

SIDE
MIC -IN

SIDE
HP - OUT

DEBUG
PORT

TPM

SIO ITE8772

PS/2 KB

PS/2 Mouse

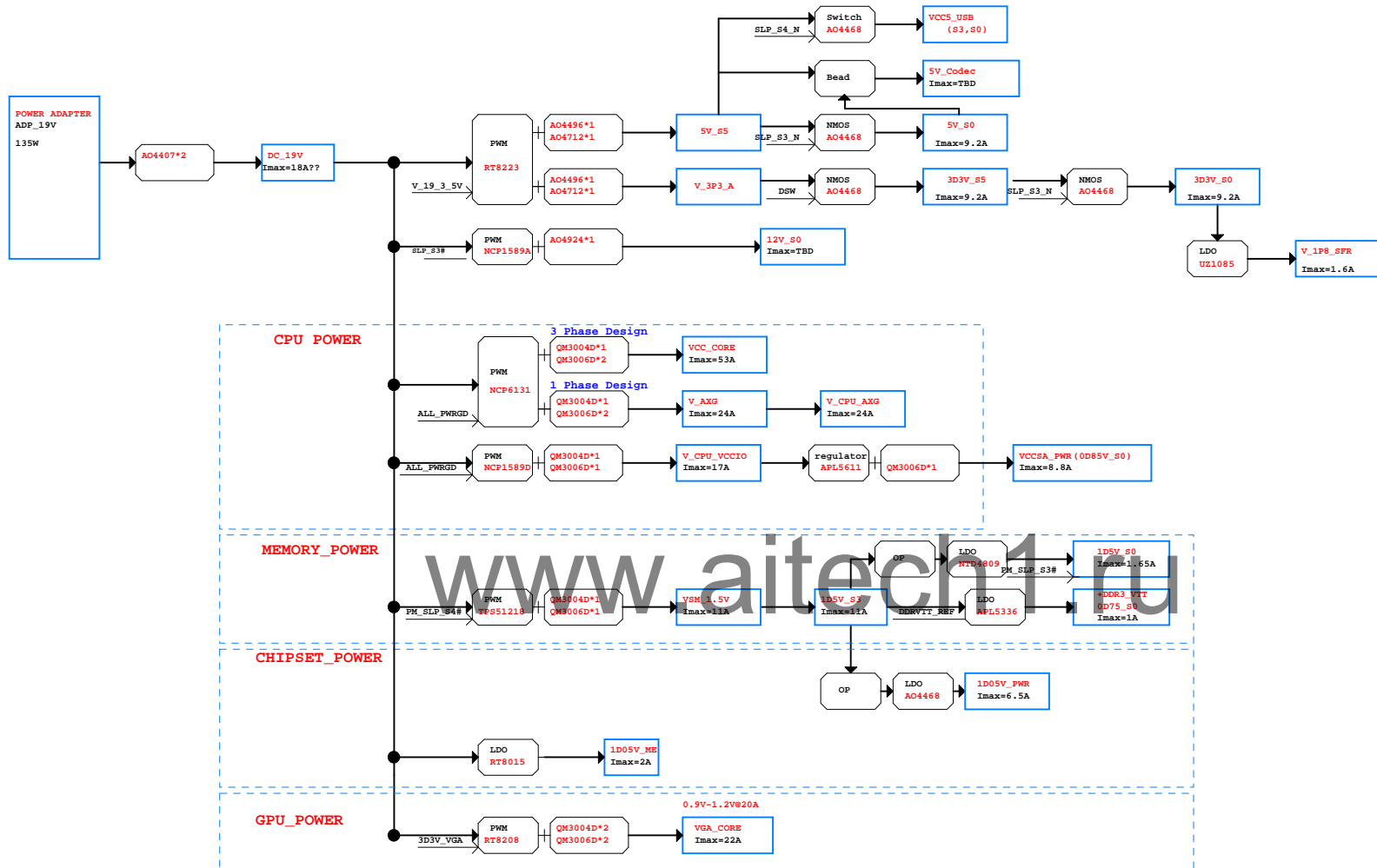
CPU 1X4 FAN

GPU 1X4 FAN

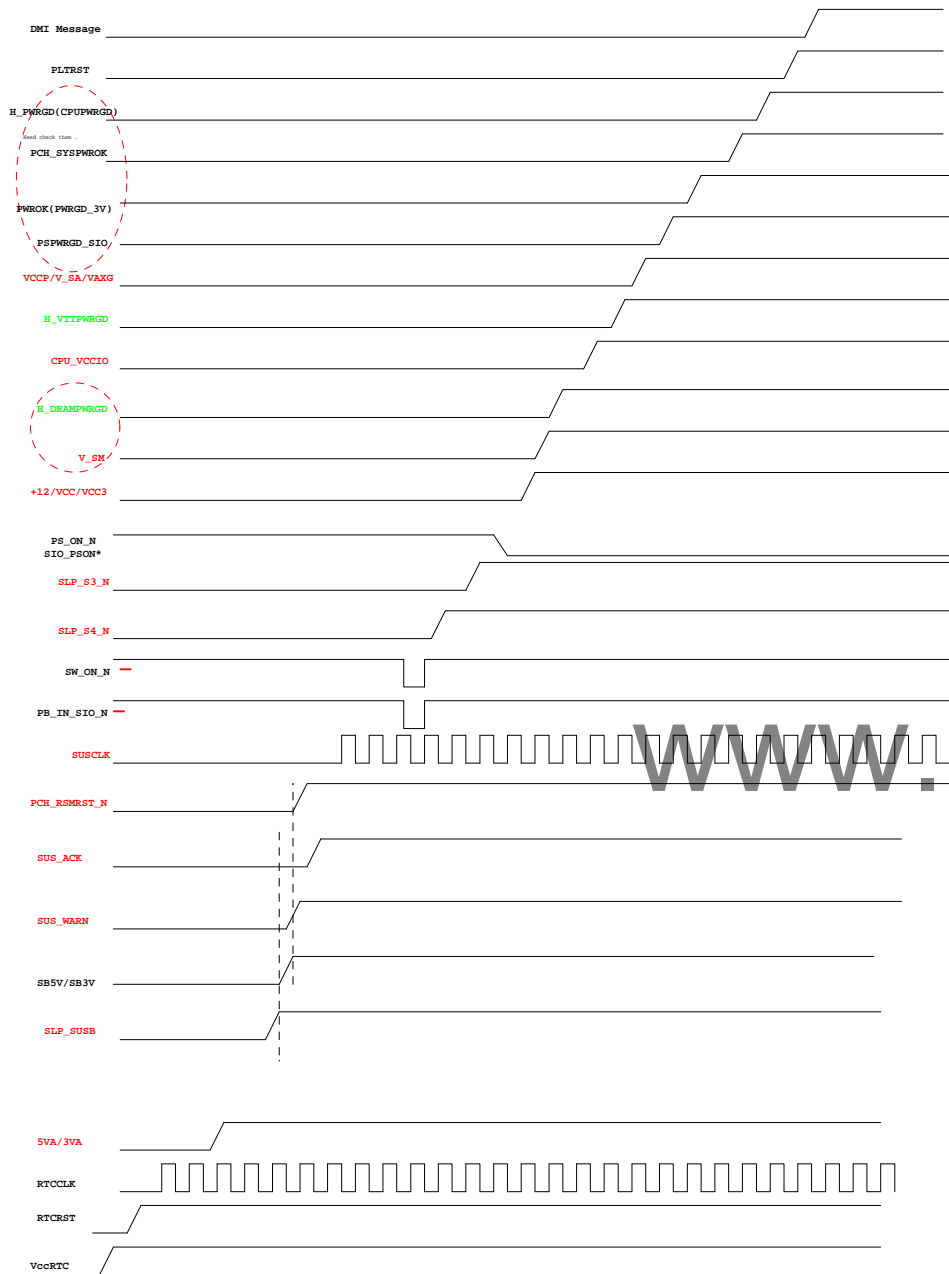
wistron

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsinchu, Taipei

Title
Size C Document Number Zappa Rev SA
Date: Sunday, January 02, 2011 Sheet 2 of 52

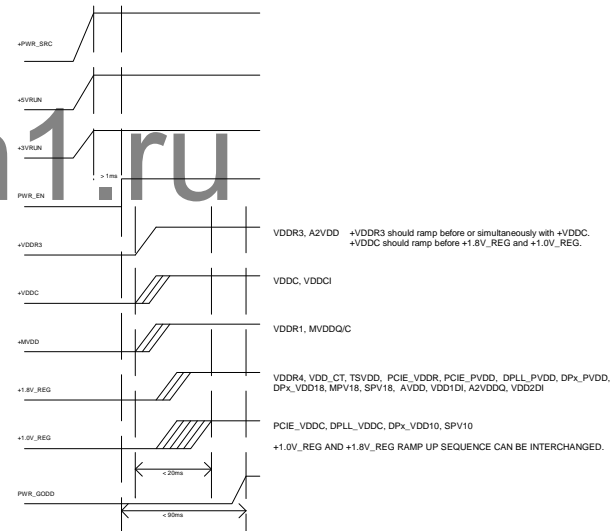


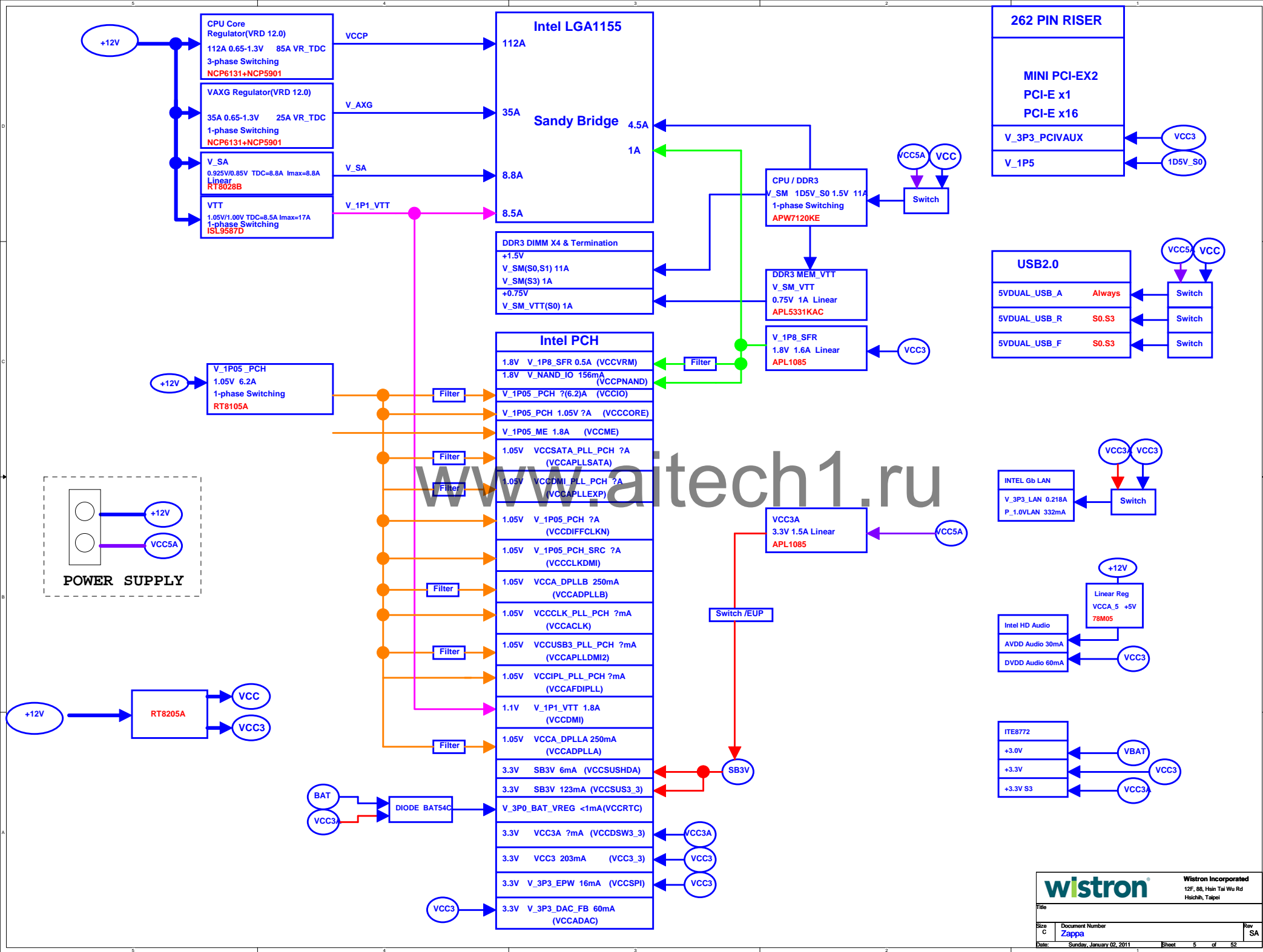
POWER ON SEQUENCE

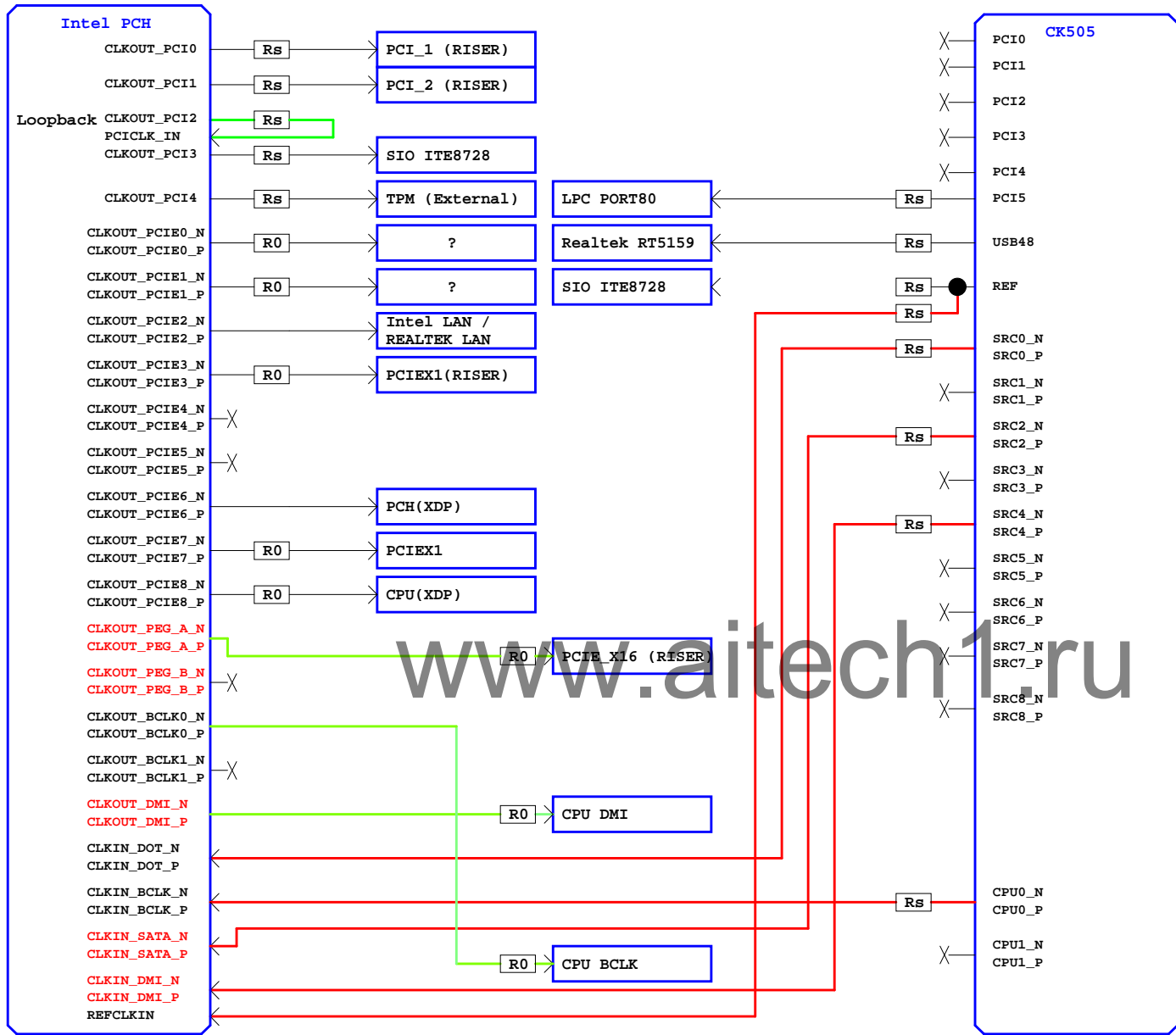


GPU CEDAR POWER SEQUENCE

POWER UP SEQUENCE (not to scale)







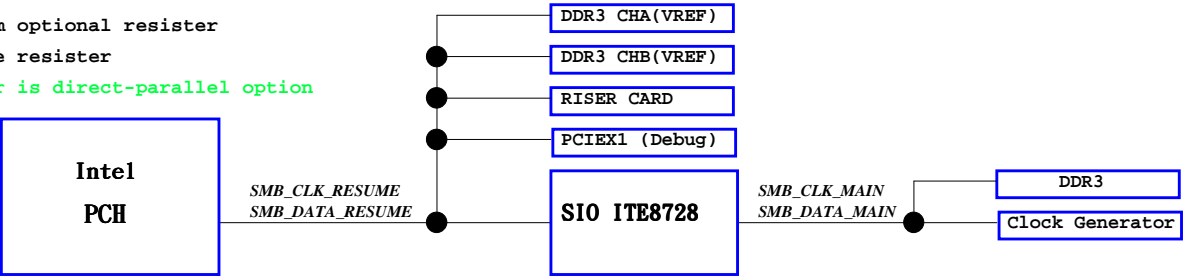
BTM: Buffer Through Mode
 Need CK505 to provide 4 clock to PCH
 FCIM: Full Clock Intergration Mode
 Remove CK505

Note: Red Color is Gen2 spec.


Note: R0 is 0 ohm optional resister

Note: Rs is serie resister


Note: Green Color is direct-parallel option

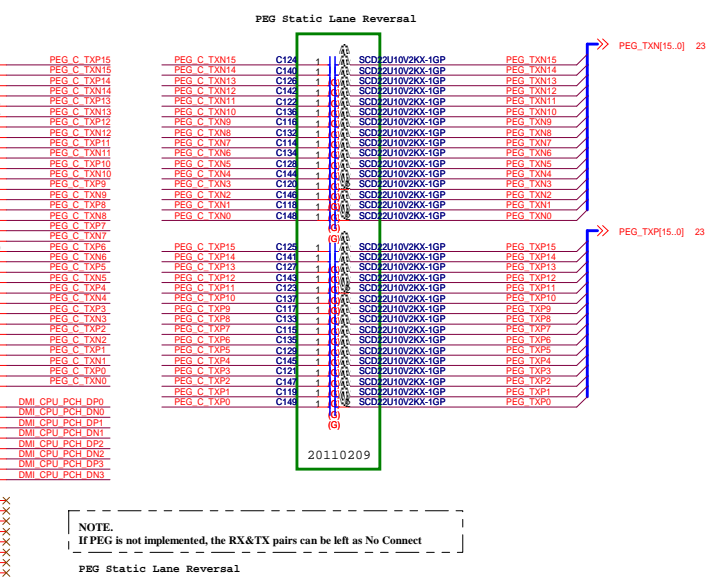
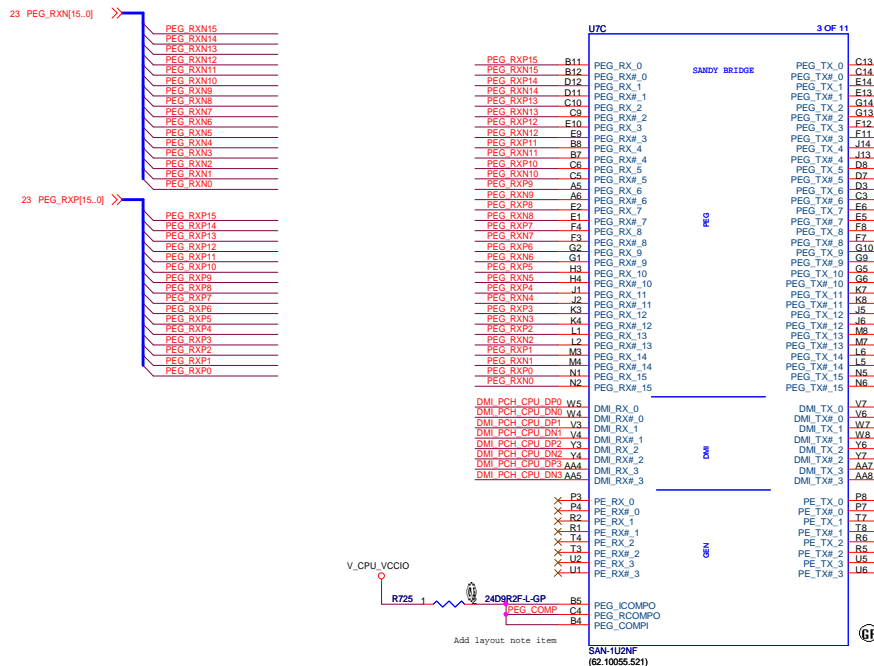
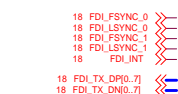


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Title CLOCK GEN			
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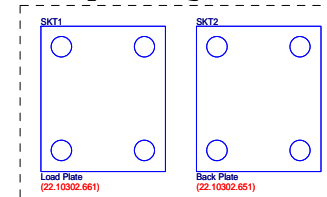
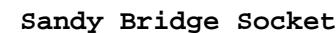
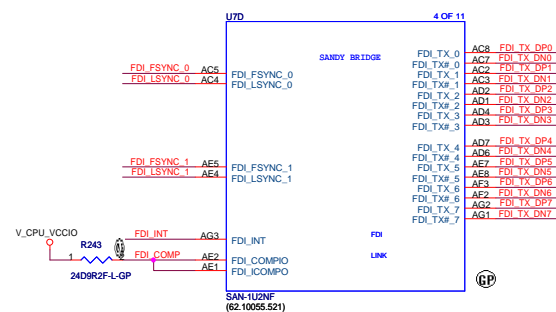
		Wistron Incorporated 12F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title RESERVE			
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NOTE.
If PEG is not implemented, the RX&TX pairs can be left as No Connect

PEG Static Lane Reversal








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15 M_DATA_A[0..63] <<>
16 M_DATA_B[0..63] <<>

15 M_DQS_A_DP[0..7] <<>
15 M_DQS_A_DN[0..7] <<>

16 M_DQS_B_DP[0..7] <<>
16 M_DQS_B_DN[0..7] <<>

15	M_MAA_A[0:15]	
16	M_MAA_B[0:15]	
15	M_WE_A_N	
15	M_CAS_A_N	
15	M_RAS_A_N	
15	M_SBS_A0	
15	M_SBS_A1	
15	M_SBS_A2	
16	M_WE_B_N	
16	M_CAS_B_N	
16	M_RAS_B_N	
16	M_SBS_B0	
16	M_SBS_B1	
16	M_SBS_B2	

```

15 M_SCS_A_N0
15 M_SCS_A_N1
15 M_SCKE_A0
15 M_SCKE_A1

15 M_ODT_A0
15 M_ODT_A1

16 M_SCS_B_N0
16 M_SCS_B_N1
16 M_SCKE_B0
16 M_SCKE_B1
16 M_ODT_B0
16 M_ODT_B1

```

15 CK_M_DDR0_A_DP 

15 CK_M_DDR0_A_DN 

15 CK_M_DDR1_A_DP 

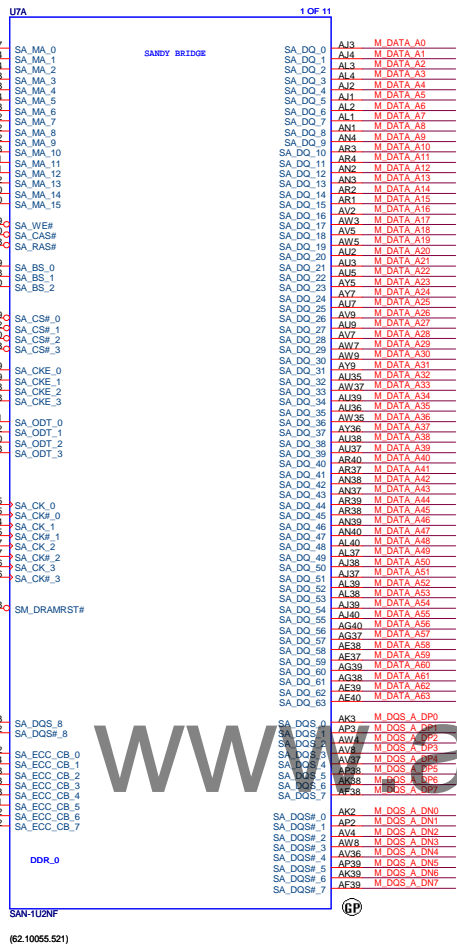
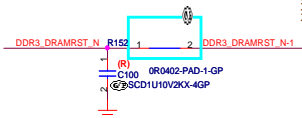
15 CK_M_DDR1_A_DN 

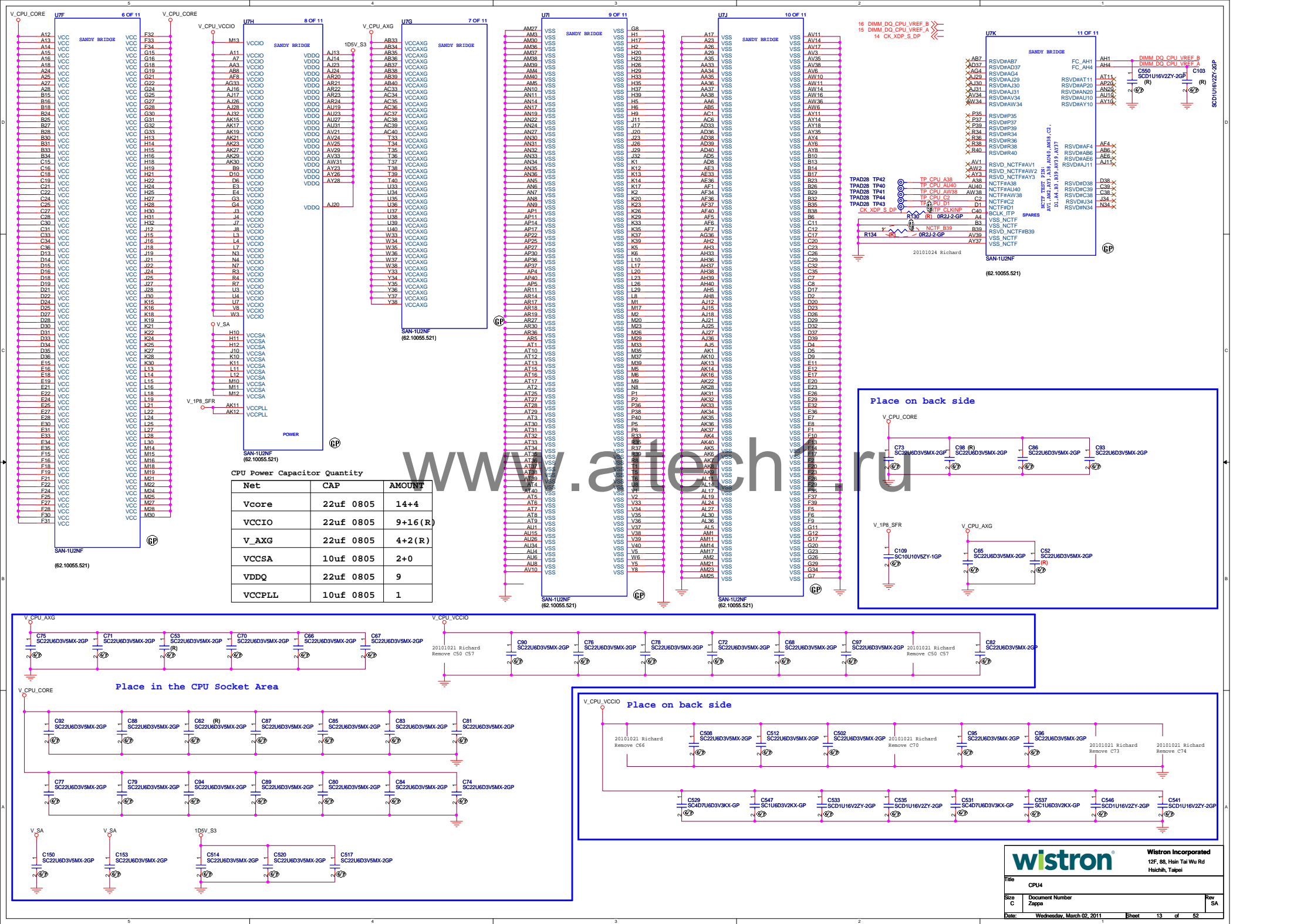
16 CK_M_DDR0_B_DP 

16 CK_M_DDR0_B_DN 

16 CK_M_DDR1_B_DP 

16 CK_M_DDR1_B_DN 

15,16 DDR3_DRAMRST_N <<-



XDP(ITP) for CPU

17,44 CPU_CORE_PWRGD >>

10 H_TDO >>

10 H_TDI >>

10 H_TMS >>

10 H_TCK >>

10 H_TRST_N >>

10 H_CPUVST_N >>

10 H_PWD_N >>

10 H_PWDY_N >>

10,17 H_PWRGD >>

17,31,32 SIO_PWNBTN_N >>

10,17,23,31 PLT_RST_N >>

15,16,17,23,28,47 SMB_DATA_MAIN >>

15,16,17,23,28,47 SMB_CLK_MAIN >>

10,17 XDP_DBRESET_N >>

10 H_BPMH0 >>

10 H_BPMH1 >>

10 H_BPMH2 >>

10 H_BPMH3 >>

10 H_BPMH4 >>

10 H_BPMH5 >>

10 H_BPMH6 >>

10 H_BPMH7 >>

18 CK_100M_CPU_XDP_DN >>

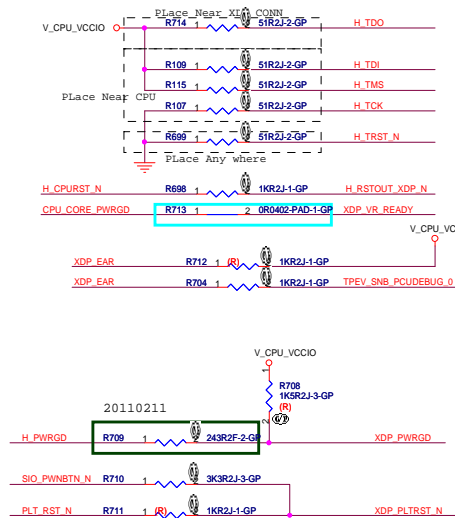
18 CK_100M_CPU_XDP_DP >>

13 CK_XDP_S_DP >>

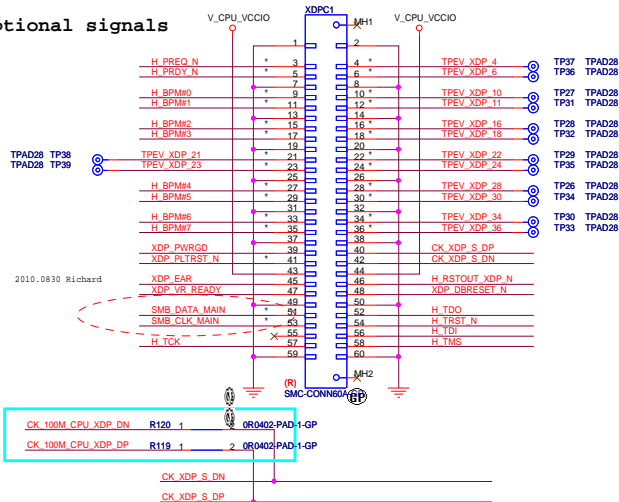
10 CK_XDP_S_DN >>

10 TPEV_SNB_PCUDEBUG_0 <<

XDP(ITP) for CPU



* : Optional signals



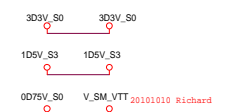
All parts can be placed at back side

CRT Header for Debug

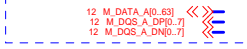
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20101102 Richard
Remove XDN RGB

20101027 Richard
DEL DBRST VDR DDC_CLK DATA



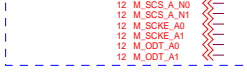
DDR DATA



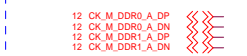
DDR CMD/ADD



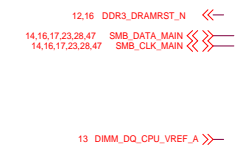
DDR CTRL



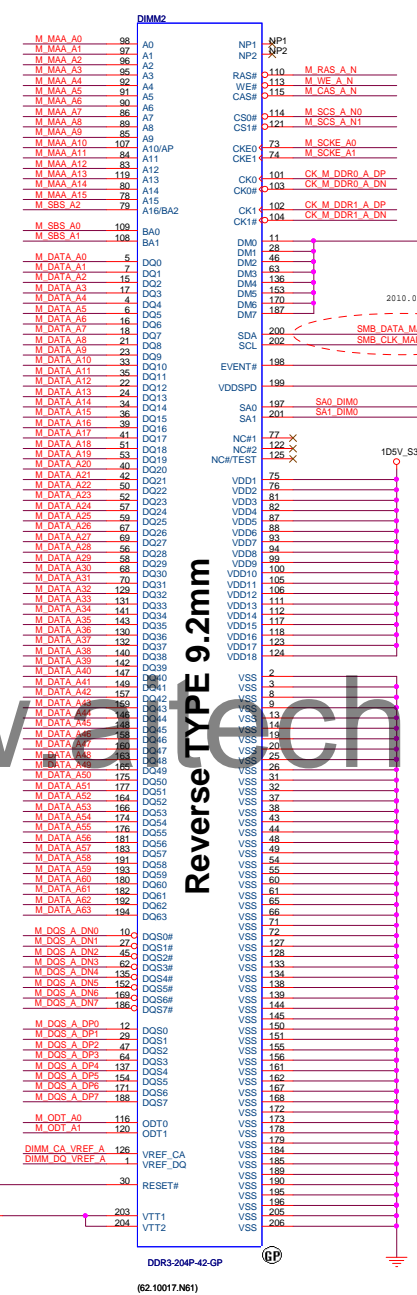
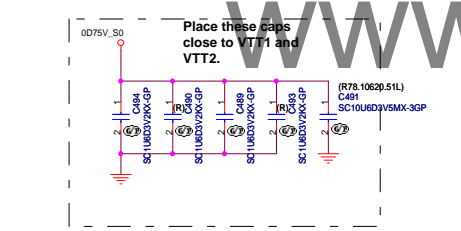
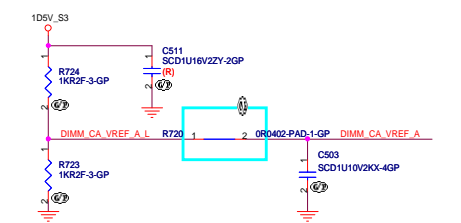
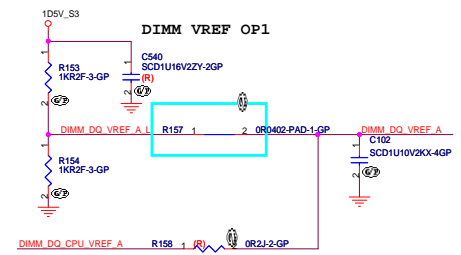
DDR CLOCK



DDR OTHERS



SSID = MEMORY



DDR DATA

12 M_DATA B[0..63]
12 M_DQS_B_DP[0..7]
12 M_DQS_B_DN[0..7]

DDR CMD/ADD

12 M_MAA_B[0..15]

12 M_WE_B_N
12 M_CAS_B_N
12 M_RAS_B_N
12 M_SBS_B0
12 M_SBS_B1
12 M_SBS_B2

DDR CTRL

12 M_SCS_B_N0
12 M_SCS_B_N1
12 M_SCKE_B0
12 M_SCKE_B1
12 M_ODT_B0
12 M_ODT_B1

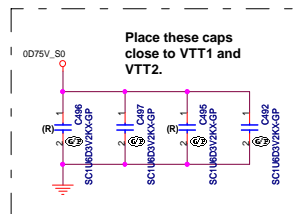
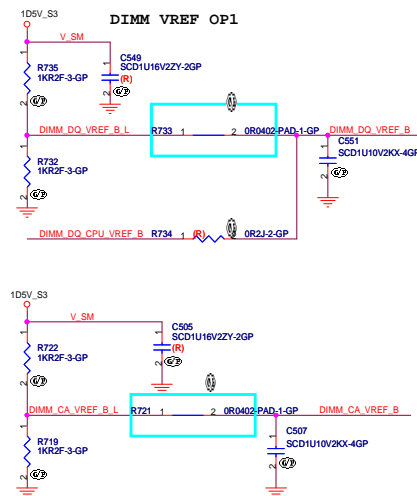
DDR CLOCK

12 CK_M_DDR0_B_DP
12 CK_M_DDR0_B_DN
12 CK_M_DDR1_B_DP
12 CK_M_DDR1_B_DN

DDR OTHERS

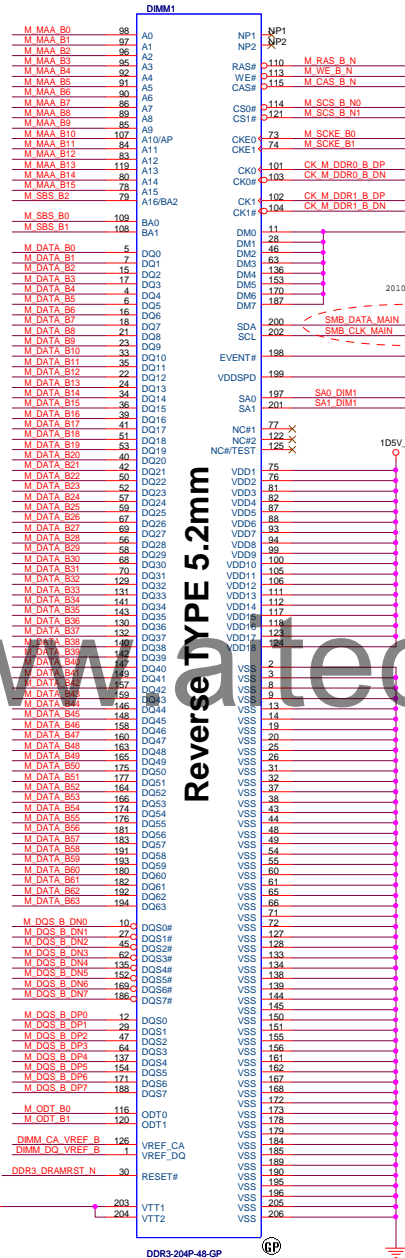
12,15 DDR3_DRAMRST_N

SSID = MEMORY



0D75V_S0

0D75V_S0



Reverse TYPE 5.2mm

H=5.2mm REV

NP1

NP2

RAS#

WE#

CAS#

CS0#

CS1#

CKE0

CKE1

CK0

CK0#

CK1

CK1#

DM0

DM1

DM2

DM3

DM4

DM5

DM6

DM7

SDA

SCL

EVENT#

VDDSPD

SA0

SA1

NC#1

NC#2

NC#3

NC#4

NC#5

NC#6

NC#7

NC#8

NC#9

NC#10

NC#11

NC#12

NC#13

NC#14

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NC#256

NC#257

NC#258

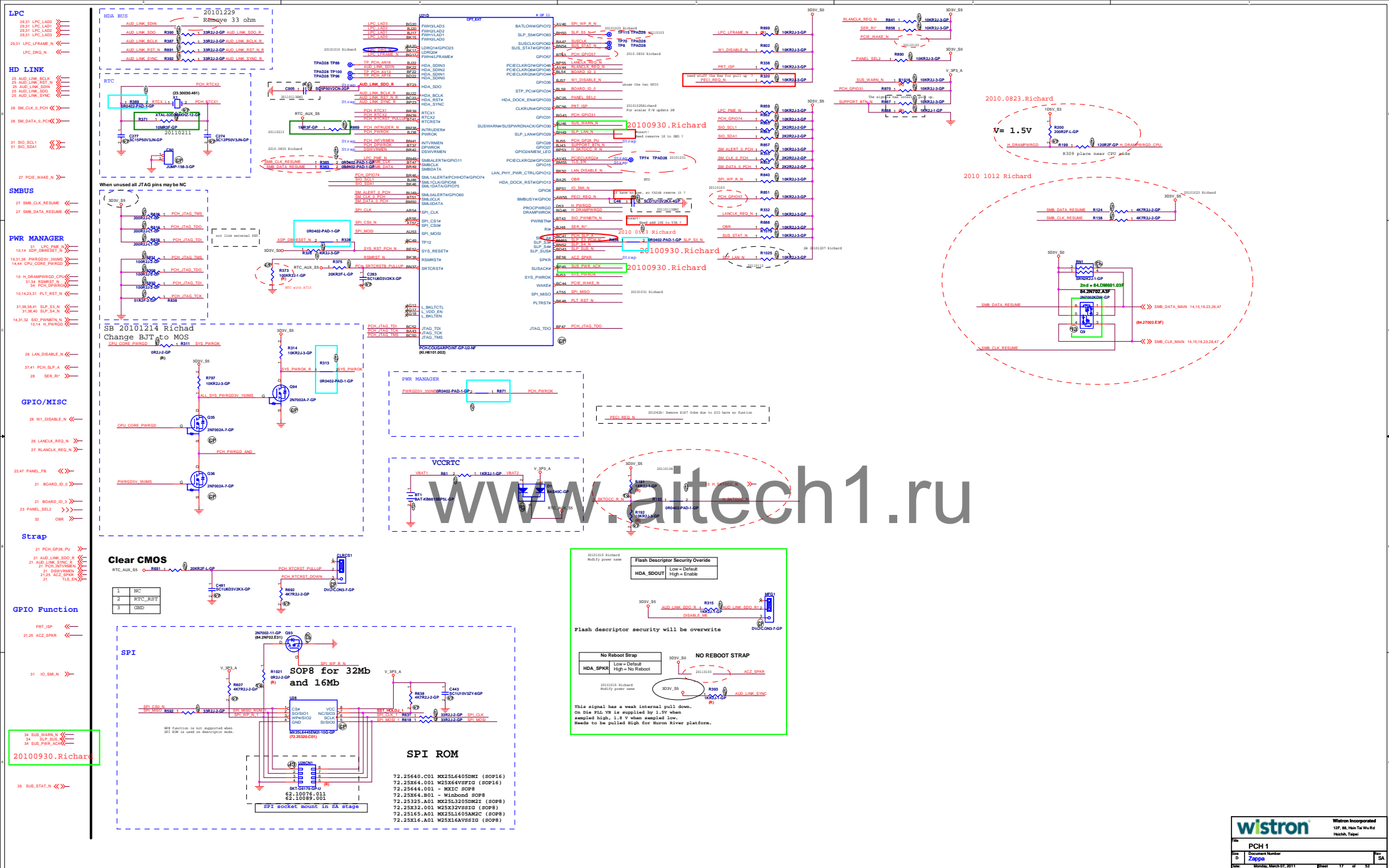
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NC#260

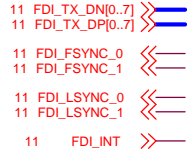
NC#261

NC#262

NC#263



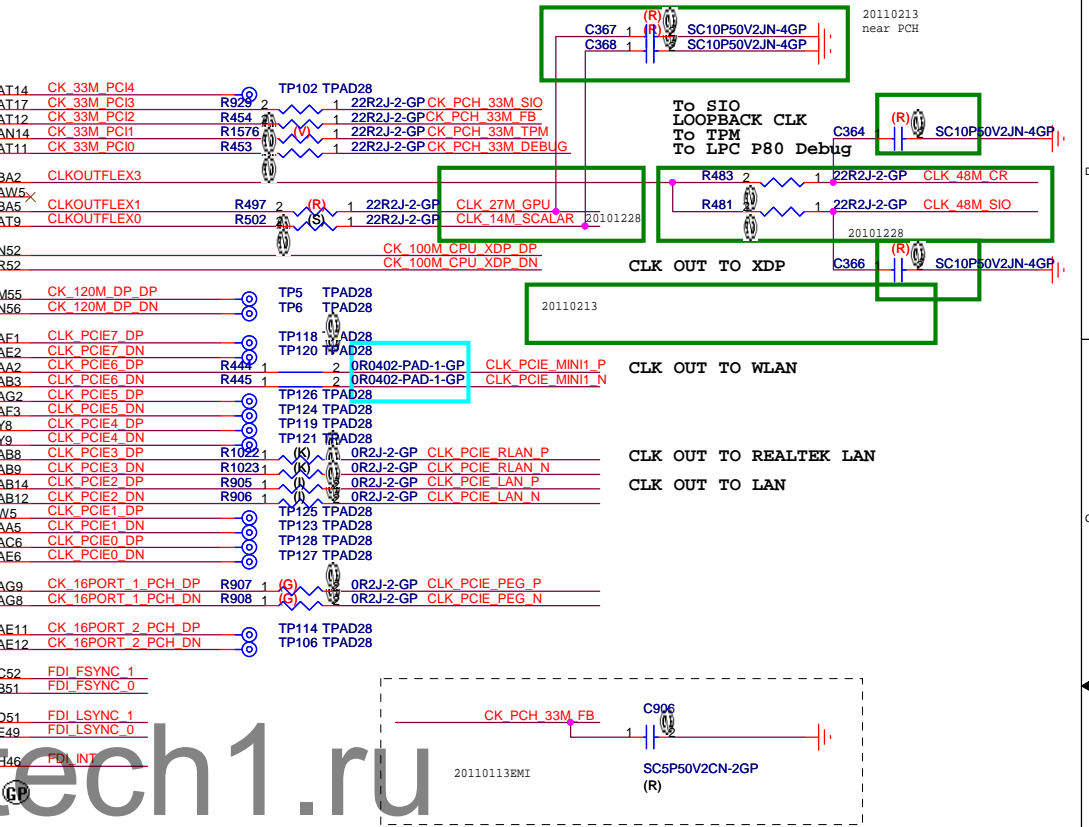
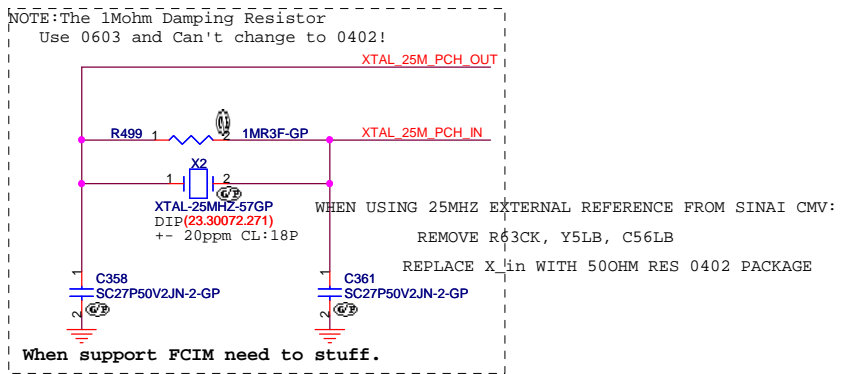
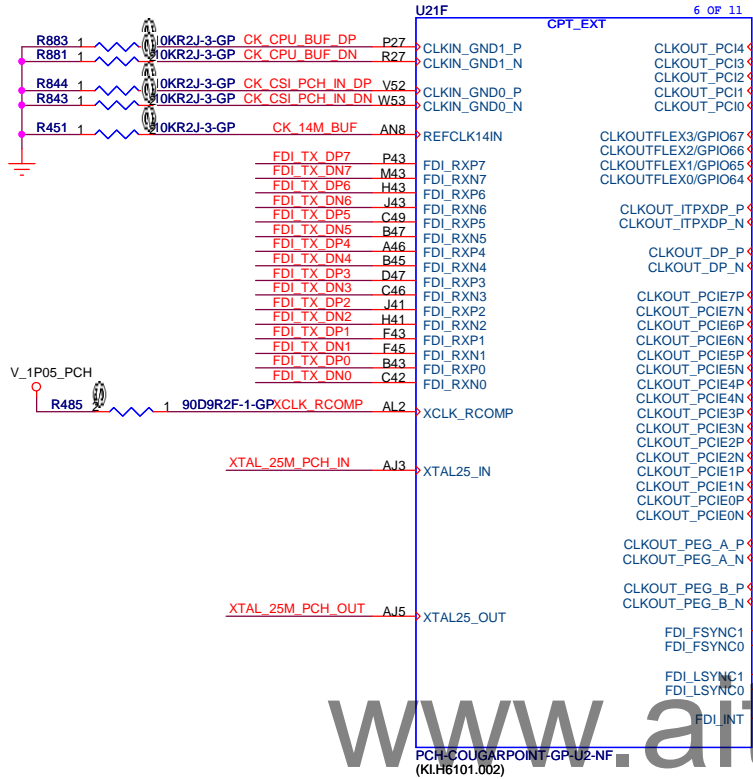
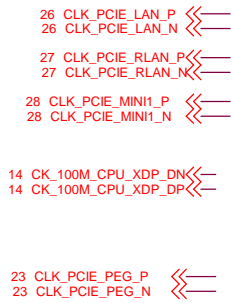
FDI




PCI CLOCK



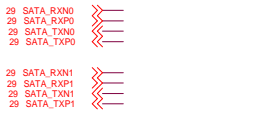
PCIE CLOCK



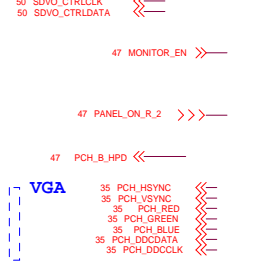
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Title PCH 2			
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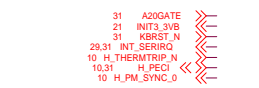
SATA



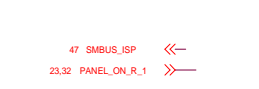
DP PORT B to SCALAR



OTHERS



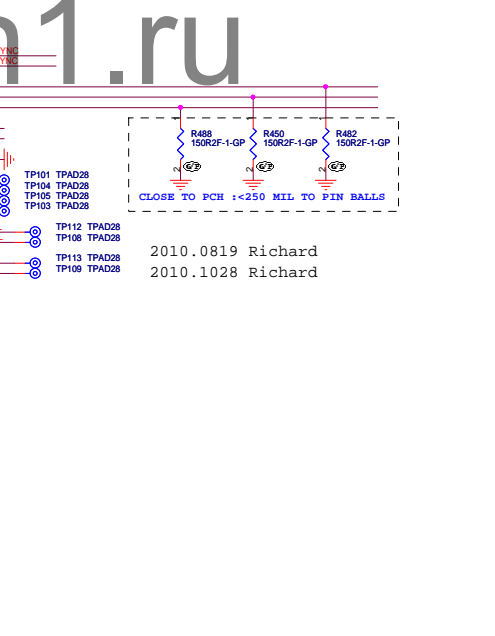
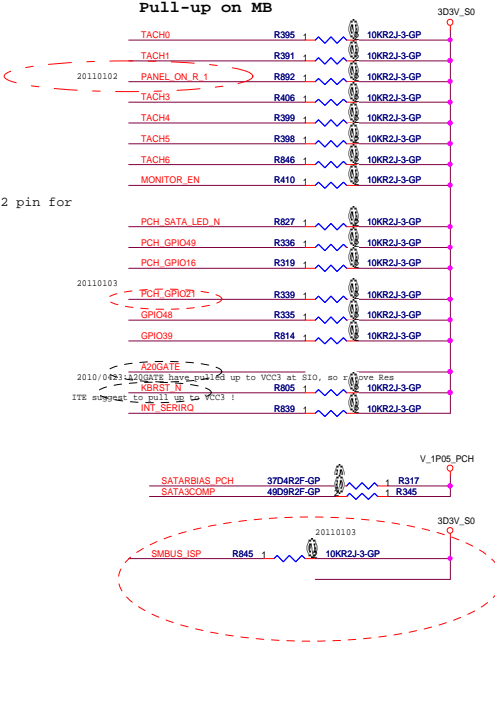
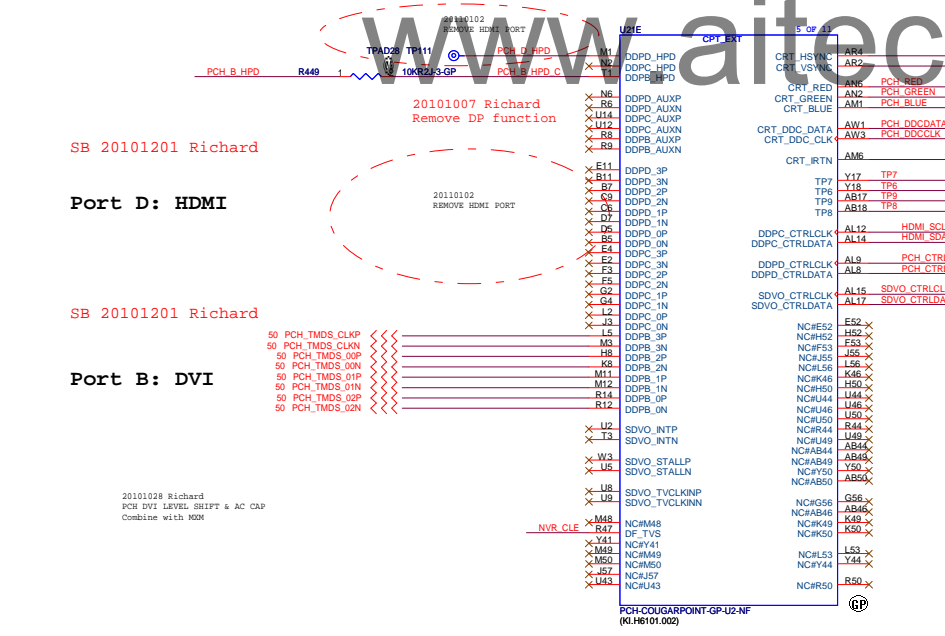
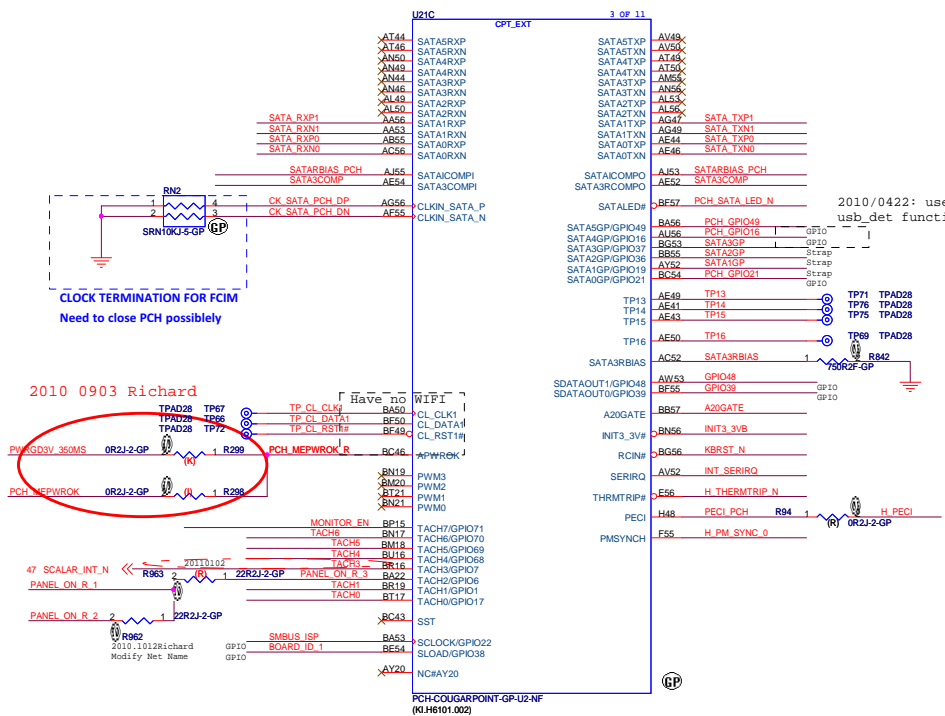
GPIO



Strap



DP PORT D

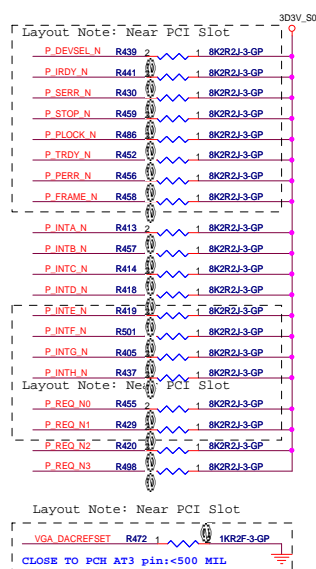
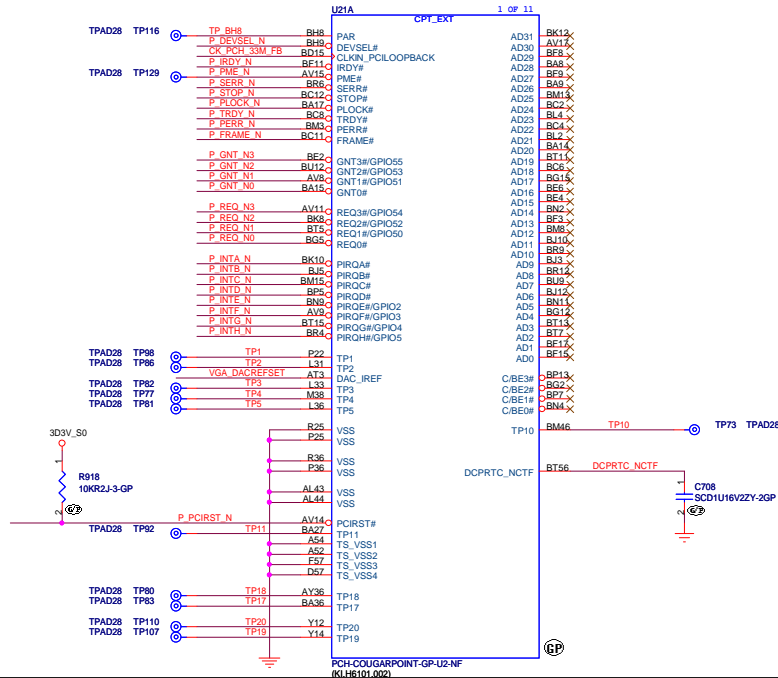


18 CK_PCH_33M_FB >>

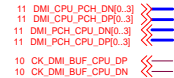
Strap



26,27 P_PCIRST_N <<—



DMI



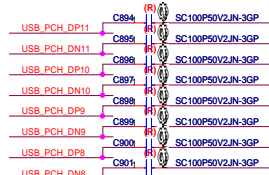
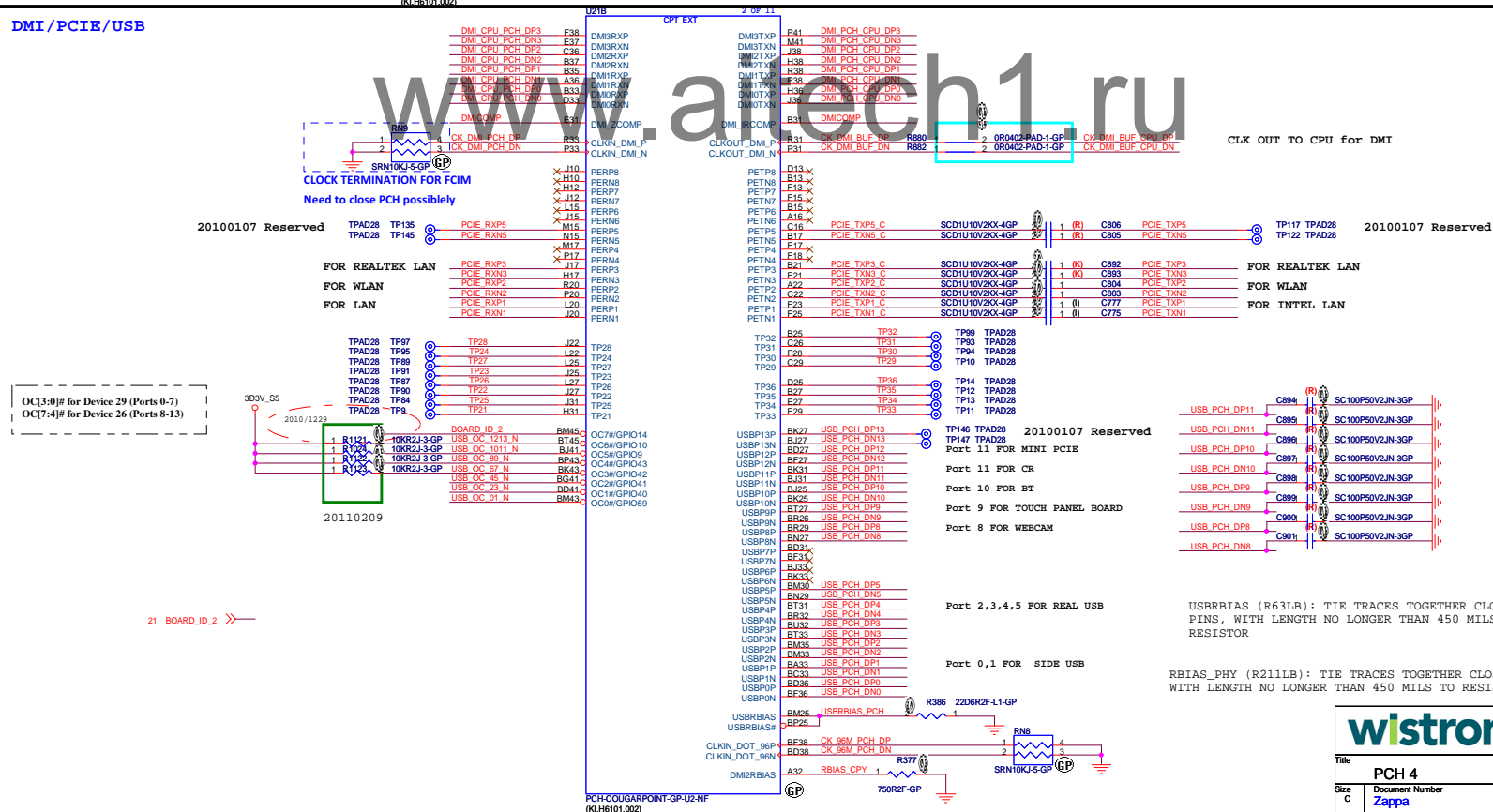
26	PCIE_RXP1	
26	PCIE_RXN1	
26	PCIE_TXP1	
26	PCIE_TXN1	
28	PCIE_RXP2	
28	PCIE_RXN2	
28	PCIE_TXP2	
28	PCIE_TXN2	

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30 USB_PCH_DP0
30 USB_PCH_DN0
30 USB_PCH_DP1
30 USB_PCH_DN1

30 USB_PCH_DP2
30 USB_PCH_DN2
30 USB_PCH_DP3
30 USB_PCH_DN3
30 USB_PCH_DP4
30 USB_PCH_DN4
30 USB_PCH_DP5
30 USB_PCH_DN5

```



Port 2,3,4,5 FOR REAL USB

Port 0,1 FOR SIDE USE

RBIAS_PHY (R211LB): TIE TRACES TOGETHER CLOSE TO PINS,
WITH LENGTH NO LONGER THAN 450 MILS TO RESISTOR

STRAP

```

17,25 ACZ_SPKR >>—
19 INIT3_3VB <<—
20 P_GNT_N3 <<—
17 PCH_INTVRMEN <<—
20 P_GNT_N2 <<—
20 P_GNT_N1 <<—
20 P_GNT_N0 <<—

```

```

17      TLS_EN    >>—
17  AUD_LINK_SDO_R <<—
17  AUD_LINK_SYNC_R <<—
10      H_SNB_N   >>—

```

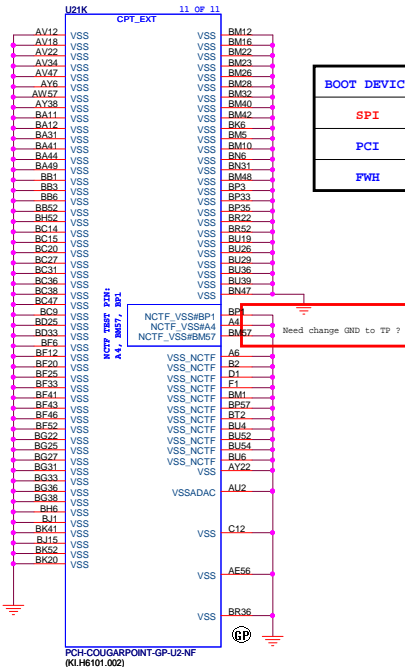
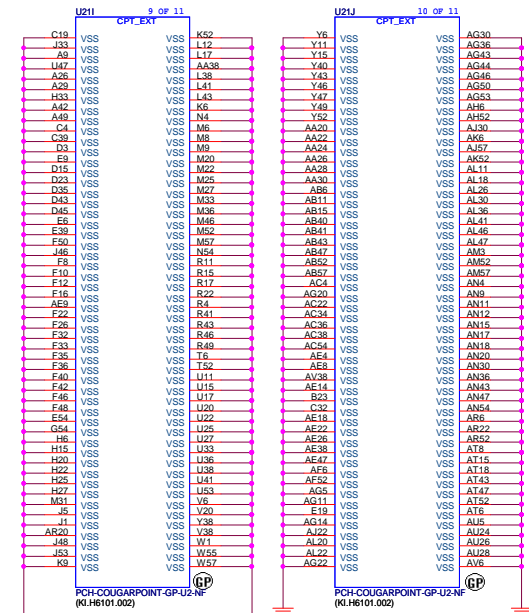
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19 SATA1GP      <<—
19  SATA2GP      <<—
19  SATA3GP      <<—
17 DSWVRMEN     <<—

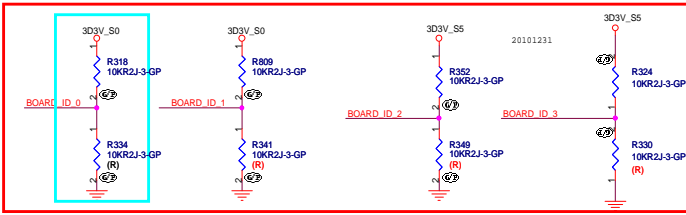
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BOARD ID

```
17 BOARD_ID_0 <<-
19 BOARD_ID_1 <<-
20 BOARD_ID_2 <<-
17 BOARD_ID_3 <<-
```



BOOT DEVICE	GNT1	SATA1GP /GPIO19
SPI	1	1
PCI	1	0
FWH	0	0



Board ID (Page17,19)

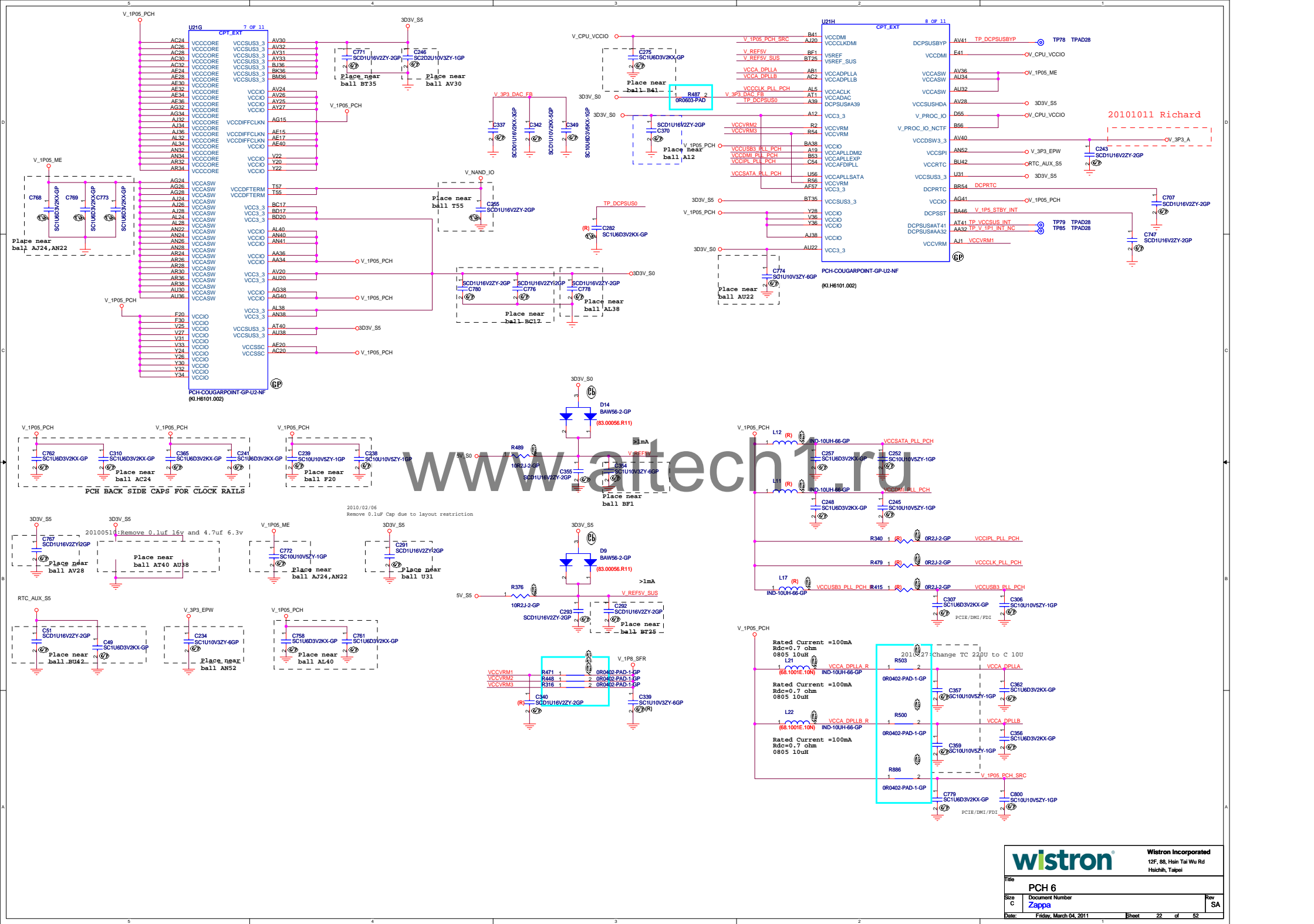
	PULL HIGH	PULL LOW
BOARD_ID_0	GPU SKU	UMA with Scalar SKU
BOARD_ID_1		
BOARD_ID_2		
BOARD_ID_3		

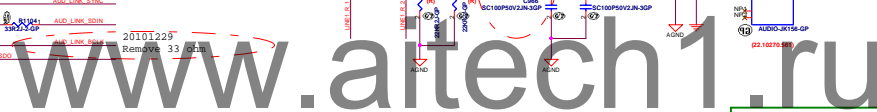
6' serial straping define

PCH Functional Straps

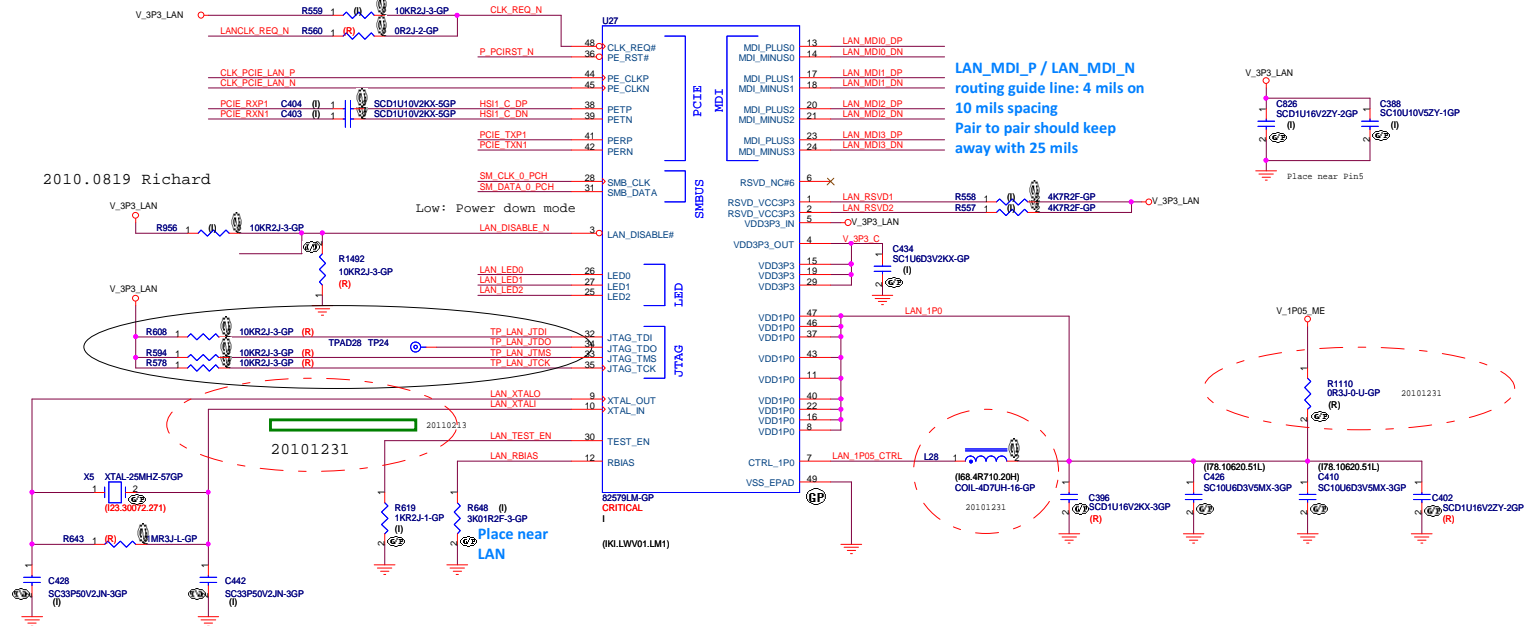
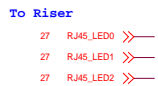
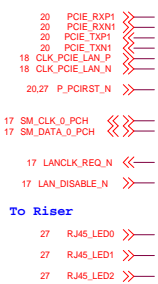
PCH EDS,Page89,Table 89-93

SPKR	The signal has a weak internal pull-down. Note: The internal pull-down is disabled after PLTRST# deasserts. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (Cougar Point will disable the TCO Timer system reboot feature). The status of this strap is readable via the NO REBOOT bit (Chipset Config Registers: Offset 3410h:Bit 5).
PCH_INTVRMEN	Integrated 1.05 V VRMs are enabled when high NOTE: This signal should always be pulled high
INIT3_3VB	This signal has a weak internal Res=20K pull-up. Note: The internal pull-up is disabled after PLTRST# deasserts. NOTE: This signal should not be pulled low
P_GNT_N3	Top-Block Swap Override The signal has a weak internal Res=20K pull-up. If the signal is sampled low, this indicates that the system is strapped to the "topblock swap" mode
P_GNT_N2	This Signal has a weak internal Res=20K pull-up. NOTE: The internal pull-up is disabled after PLTRST# deasserts. Tying this strap low configures DMI for ESI compatible operation. NOTE: ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
P_GNT_N1	Boot BIOS Destination Selection Signal has weak internal Res=20K pull-ups.
SATA1GP/GPIO19	Boot BIOS Destination Selection Signal has weak internal Res=20K pull-ups.
NVR_CLE	DMI and FDI Tx/Rx Termination Voltage The signal has a weak internal Res=20K pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts.
AUD_LINK_SDO_R	The signal has a weak internal Res=20K pull-down. Flash Descriptor Security Override Strap. In Page92 ESD.
AUD_LINK_SYNC_R	The signal has a weak internal Res=20K pull-down. On Die PLL VR is supplied by 1.5V when sampled high, 1.8 V when sampled low. In Page92 ESD.
PCH_GP28_PU	This signal has a weak internal Res=20K pull-up. NOTE: The internal pull-up is disabled after RSMRST# deasserts. The On-Die PLL voltage regulator is enabled when sampled high. When sampled low the On-Die PLL Voltage Regulator is disabled.
TLS_EN (GPIO15)	The signal has a weak internal Res=20K pull-down. NOTE: The weak internal pull-down is disabled after RSMRST# deasserts. Low = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High = Intel ME Crypto TLS cipher suite with confidentiality NOTE: A strong pull-up may be needed for GPIO functionality
DSWVRMEN	Deep S4/S5 Well On-Die Voltage Regulator Enable If strap is sampled high, the Integrated Deep S4/S5 Well (DSW) On-Die VR mode is enabled.
FB_USBF2_DET SATA2GP/GPIO36	DMI RX TERMINATION VOLTAGE OVERRIDE This signal has a weak internal Res=20K pull-down
SATA3GP SATA3GP/GPIO37	FDI RX TERMINATION VOLTAGE OVERRIDE This signal has a weak internal Res=20K pull-down

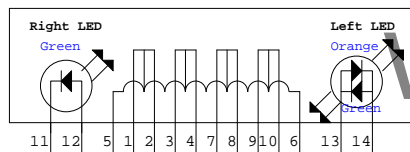




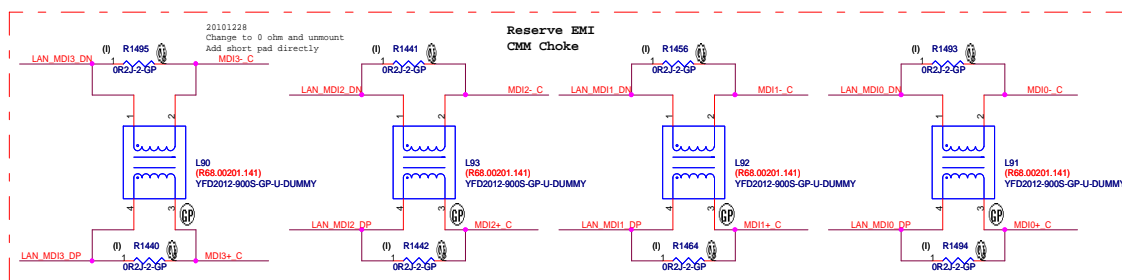
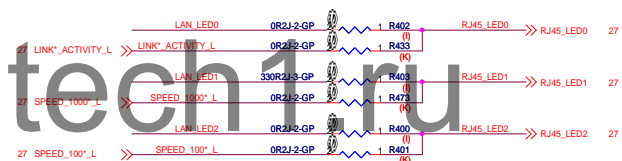
To Riser



Layout note
Keep LAN chip at least 1" from the RJ45



```
Realtek LAN: (K)
Intel LAN: (I)
```

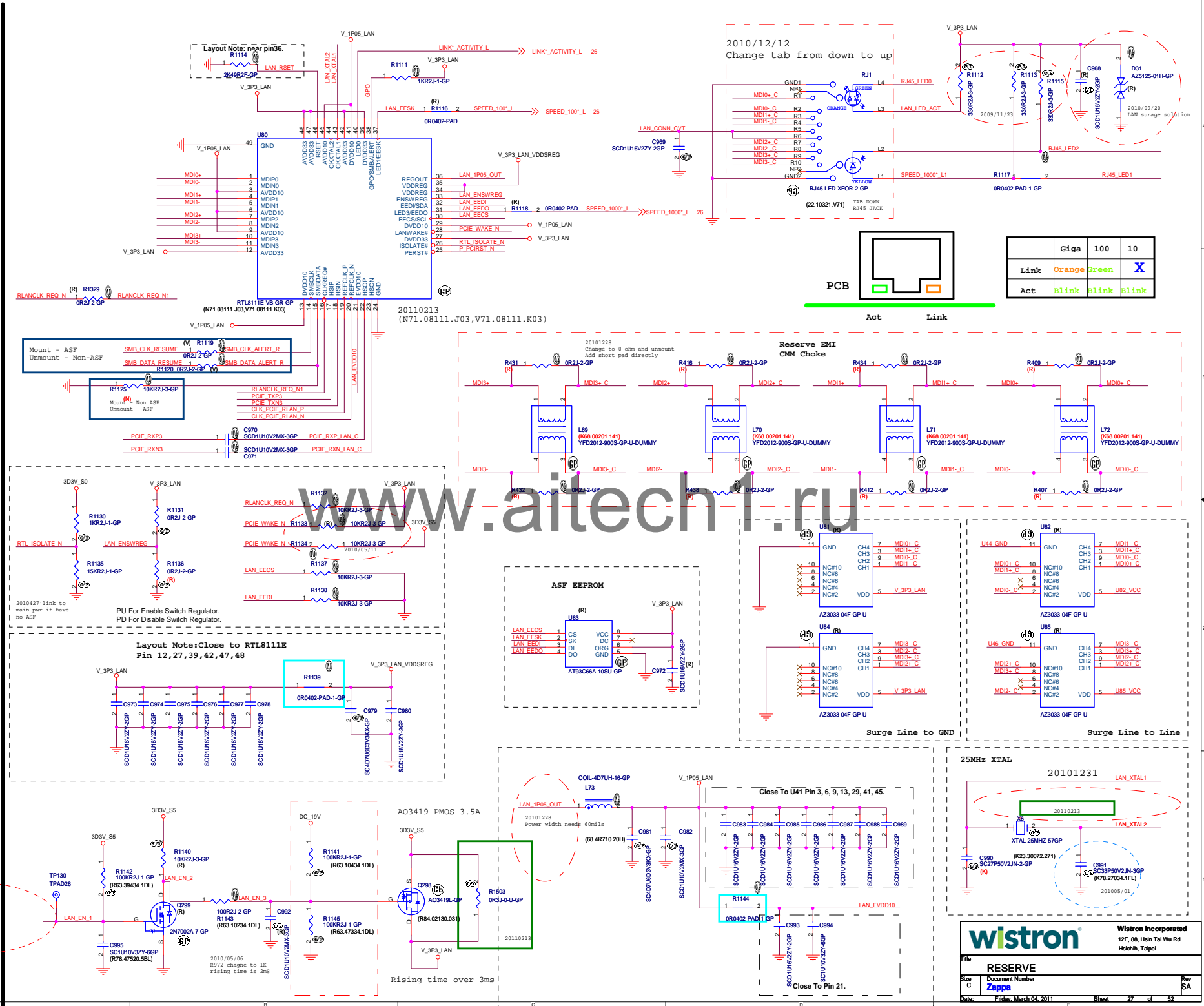
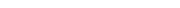
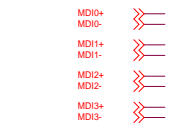
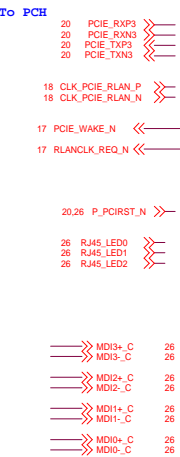


27 MD13+_C <<—
27 MD13-_C <<—

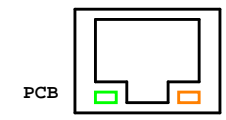
27 MD12+_C <<—
27 MD12-_C <<—

27 MD11+_C <<—
27 MD11-_C <<—

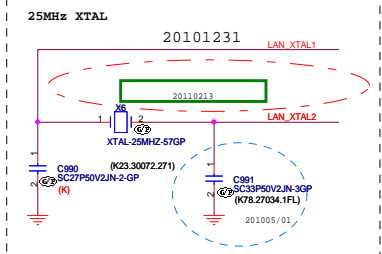
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27 MD10-_C <<—

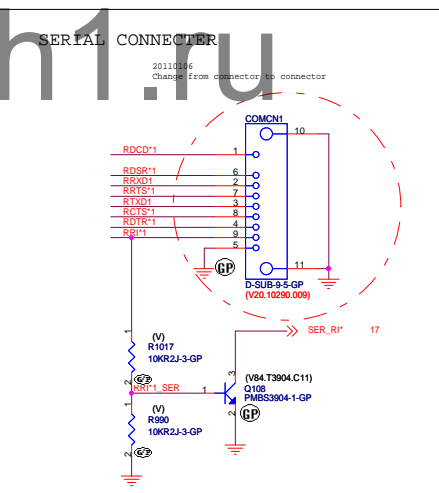
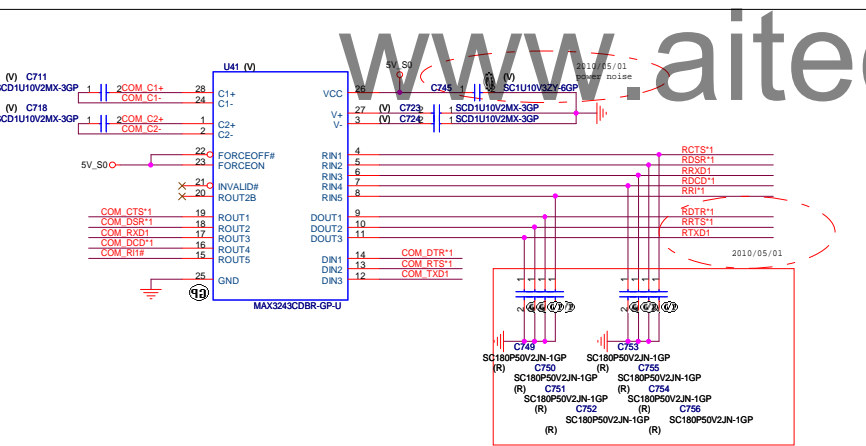
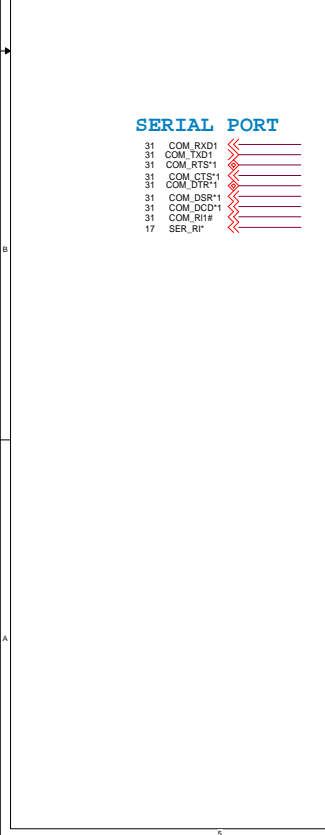
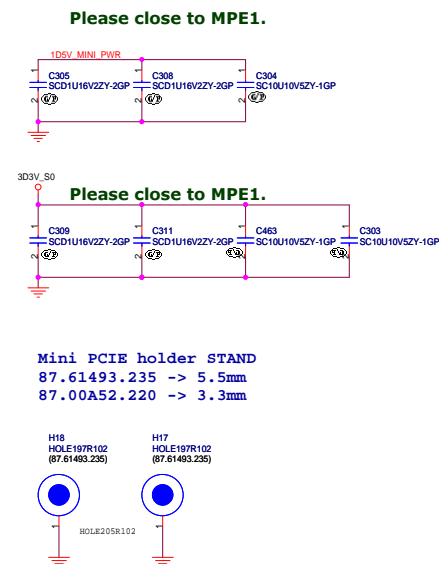
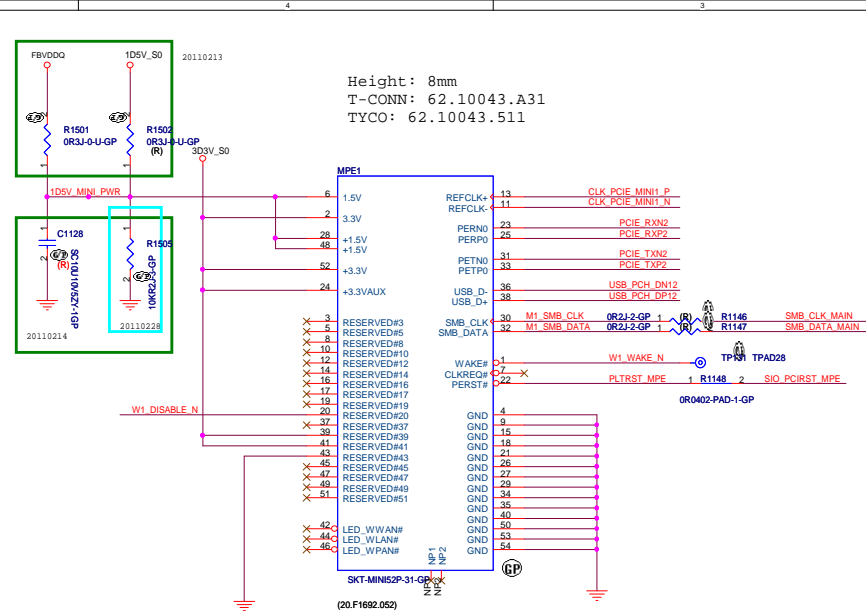
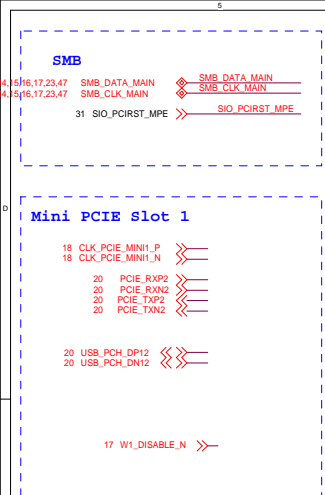


2010/12/12
Change tab from down to up



Giga	100	10
Link	Orange	Green
Act	Blink	Blink

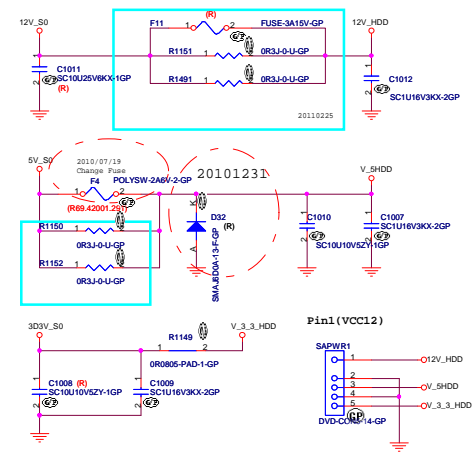
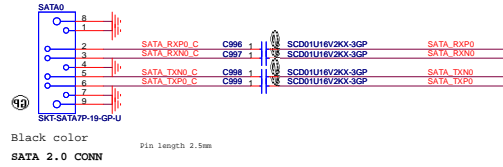




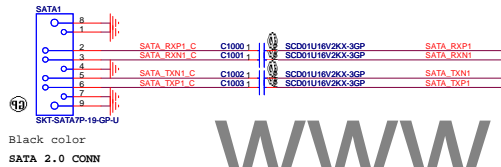
SATA HDD

PCH SATA

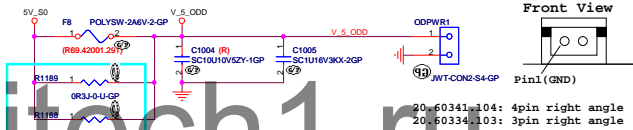
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- 19 SATA_RXP0 >>>
- 19 SATA_TXN0 >>>
- 19 SATA_TXP0 >>>
- 19 SATA_RXN1 >>>
- 19 SATA_RXP1 >>>
- 19 SATA_TXN1 >>>
- 19 SATA_TXP1 >>>
- 31 SID_PCRST_LPC >>>
- 18 CK_PCH_33M_TPM >>>
- 18 CK_PCH_33M_DEBUG >>>
- 19.31 INT_SERRIQ <<<



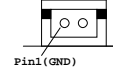
SATA ODD



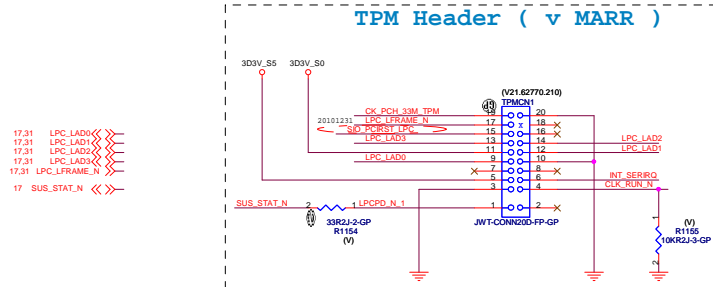
ODD SATA POWER CONNECTOR



Front View

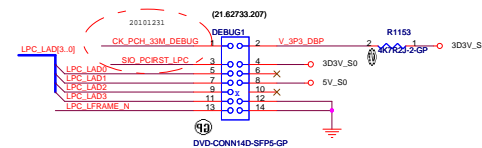


TPM Header (v MARR)



LPC DEBUG PORT

Debug Port



<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Heichih, Taipei

BTN SATA

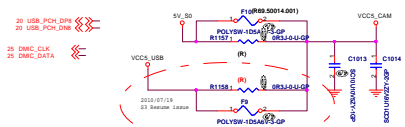
Document Number
Zappa

Date: Monday, March 07, 2011

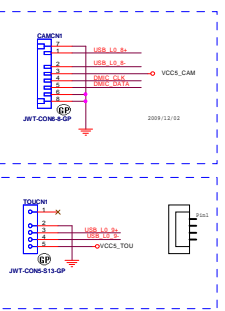
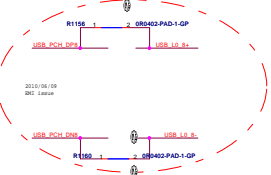
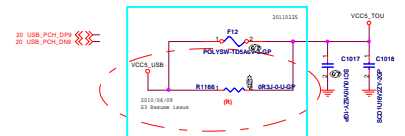
Sheet 29 of 85

Rev
SA

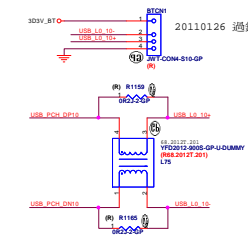
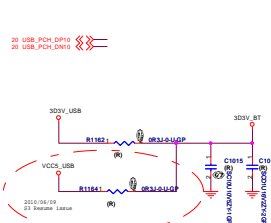
USB Port 8 -> WEB CAM



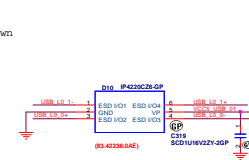
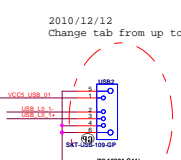
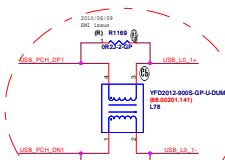
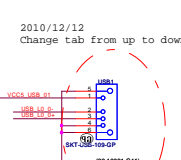
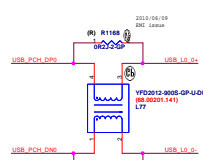
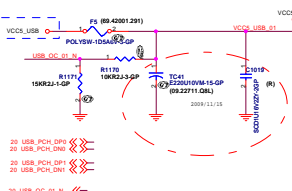
USB Port 9 -> TOUCH PANEL



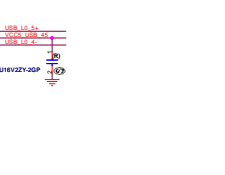
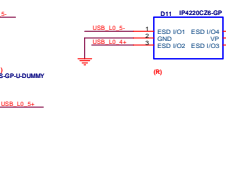
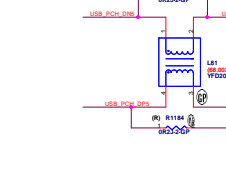
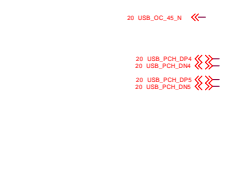
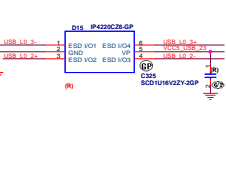
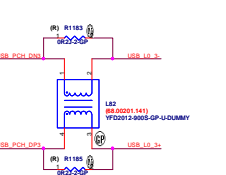
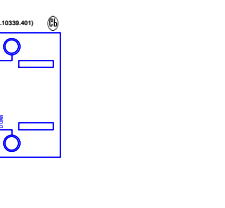
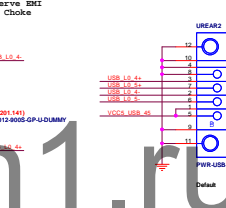
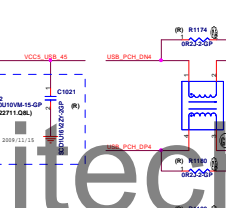
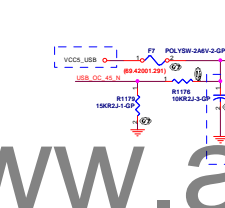
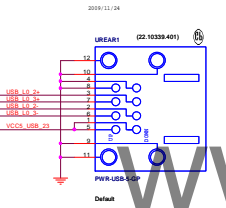
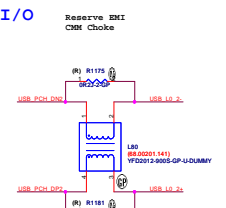
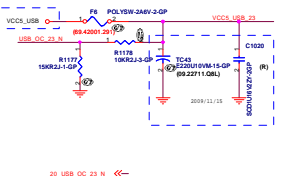
USB Port 10 -> BT



USB Port 0,1 -> SIDE I/O



USB Port 2,3,4,5 -> REAR I/O



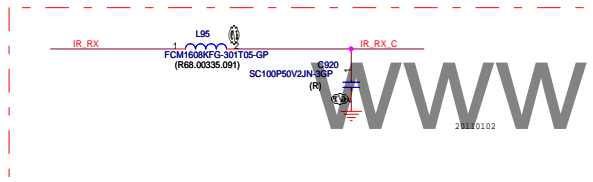
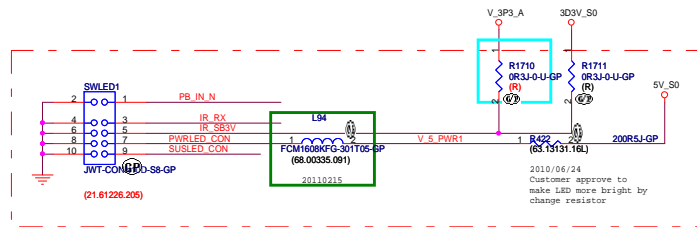
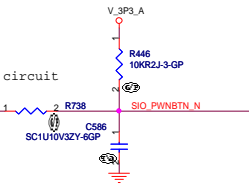
www.aitech1.ru

14,17,31 SIO_PWNBTN_N <<
 31 IR_RX_C <<
 19,23 PANEL_ON_R_1 <<
 17 OBR <<
 31 PB_IN_N <<
 31 SUSLED_N <<

POWER BUTTON

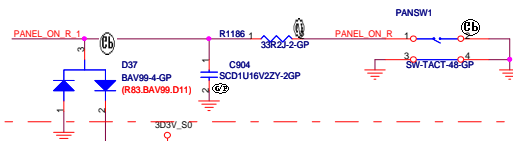
Reserve when using PCH PBN circuit

PCH internal
pullup



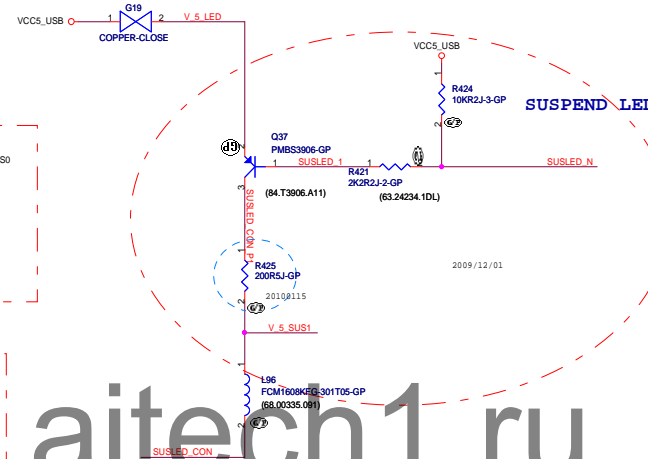
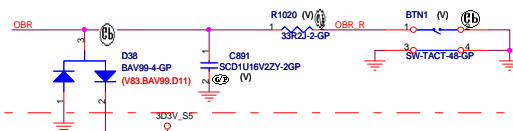
PANEL ON/OFF

20110102

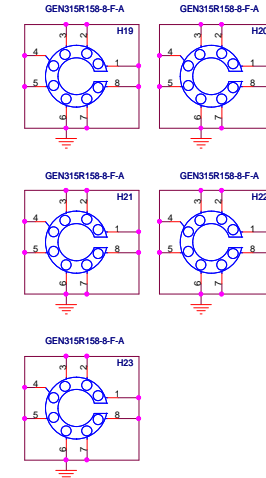


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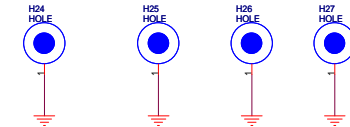
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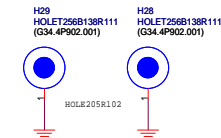
PCB MOUNTING HOLES



CPU THERMAL MODULE HOLES



GPU BLOWER STAND-OFF



<Core Design>

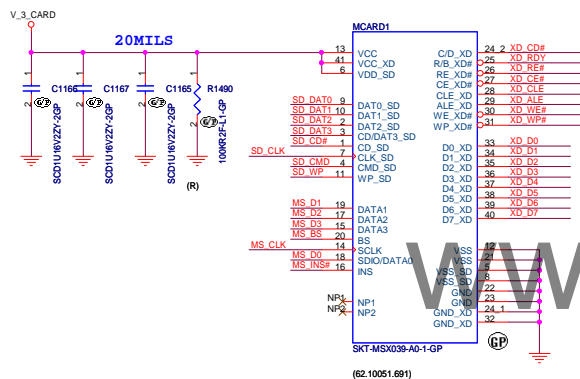
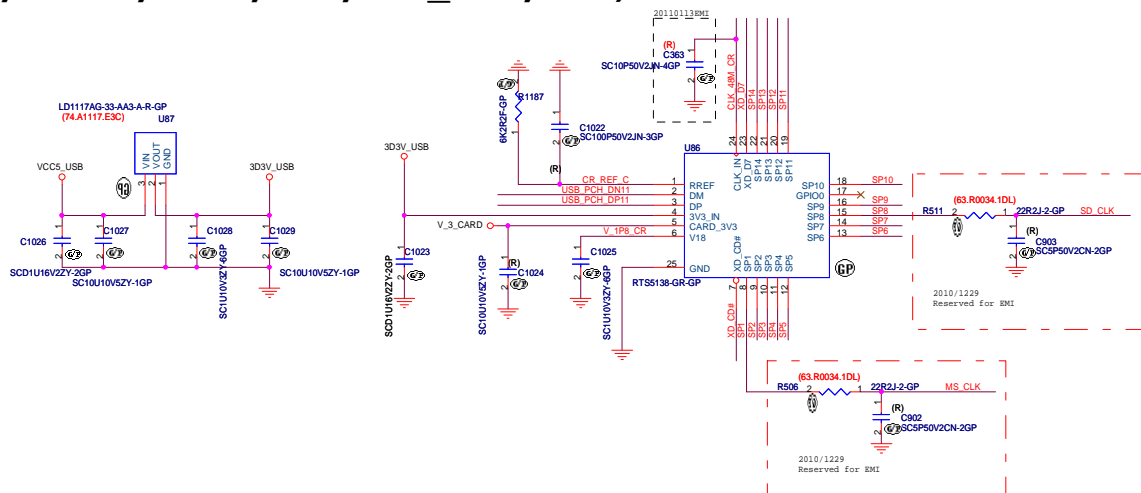
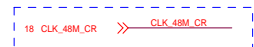
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu,
 Taipei Hsin 221, Taiwan, R.O.C.

Title		PWR SWITCH/SCREW HOLE	
Size	Document Number	Rev	
C		SA	
Date	Monday, March 07, 2011	Sheet	32 of 32

```

20 USB_PCH_DP11
20 USB_PCH_DN11

```



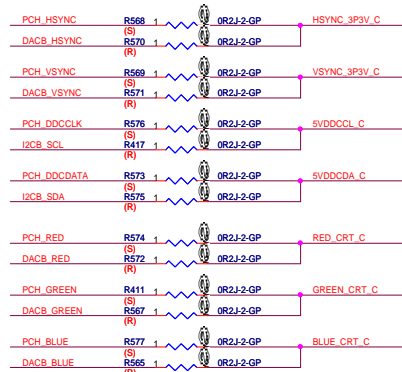
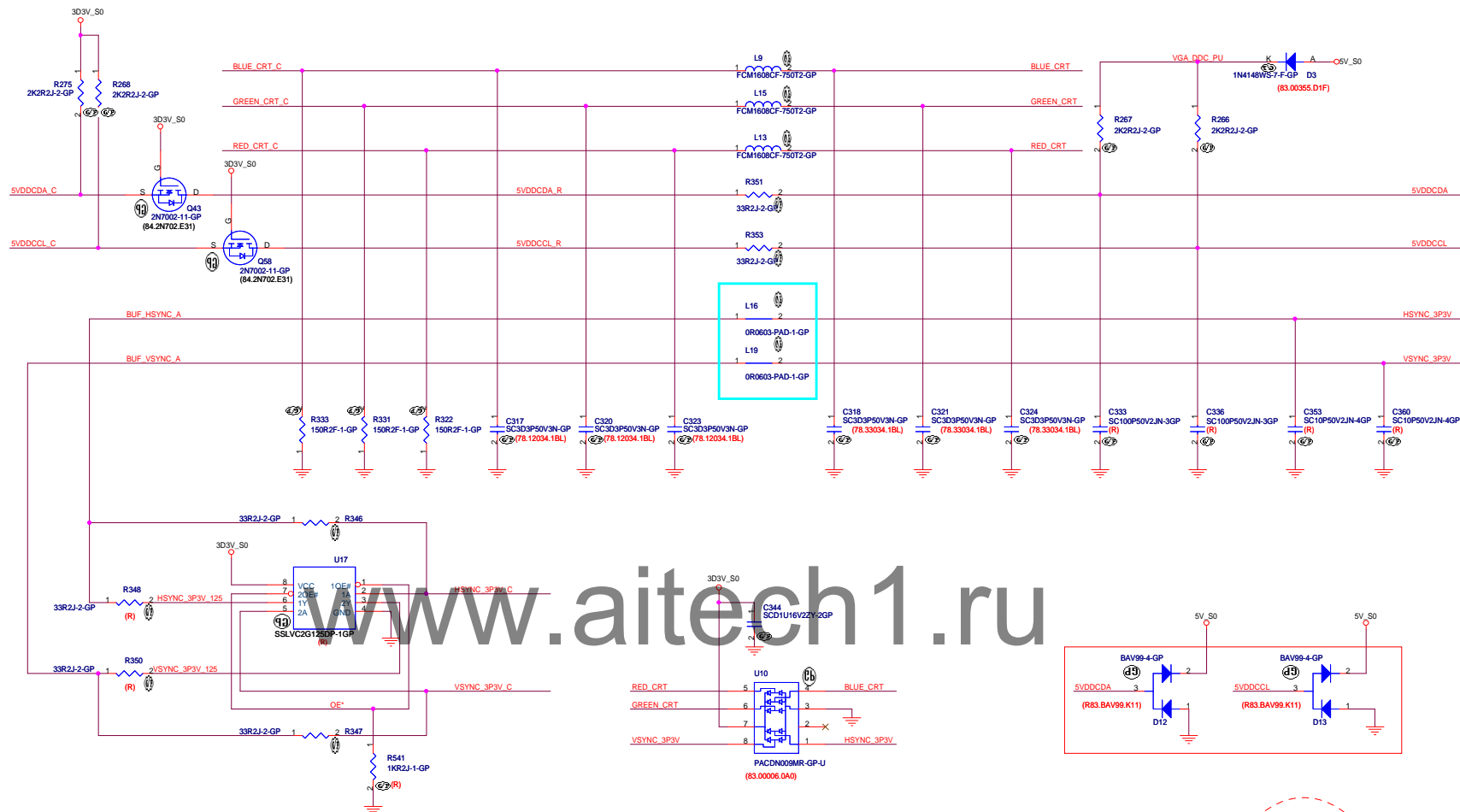
	SD_WP	MS_CLK	XD_RDY
SP2		MS_INS#	XD_RE#
SP3	SD_DAT1		XD_CE#
SP4	SD_DAT0	MS_D7	XD_CLE
SP5	SD_DAT7	MS_D3	XD_ALE
SP6	SD_CD#		XD_WE#
SP7	SD_DAT6	MS_D6	XD_WP#
	SD_CLK	MS_D2	XD_D0
SP9	SD_DAT5	MS_D0	XD_D1
SP10	SD_CMD		XD_D2
SP11	SD_DAT4	MS_D4	XD_D3
SP12	SD_DAT3	MS_D1	XD_D4
SP13	SD_DAT2	MS_D5	XD_D5
SP14		MS_D6	XD_D6

FROM GPU

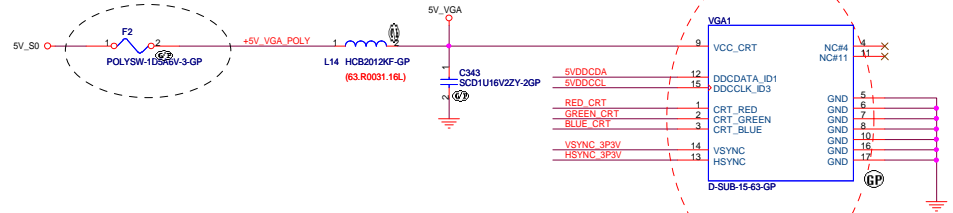
23 DACB_HSYNC
23 DACB_VSYNC
23 DACB_RED
23 DACB_GREEN
23 DACB_BLUE
23 I2CB_SCL
23 I2CB_SDA

From PCH

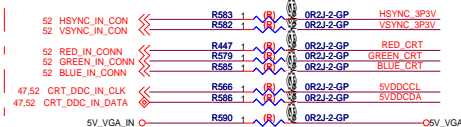
19 PCH_HSYNC
19 PCH_VSYNC
19 PCH_RED
19 PCH_GREEN
19 PCH_BLUE
19 PCH_DDCCLK
19 PCH_DDCDATA



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20110102 CLOSE TO VGA1 CONNECTOR



ATX CONNECTOR

DC-IN Connector (19V)

DC-IN Connector (19V)

2010/04/07
10uH Choke
Val: 1.68.1001C.10V

ALT: 22.10037.191

2010/04/07
10uH Choke
Val: 1.68.1001C.10V

ALT: 22.10037.191

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Val: 1.68.1001C.10V

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Val: 1.68.1001C.10V

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Val: 1.68.1001C.10V

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Val: 1.68.1001C.10V

ALT: 22.10037.191

2010/04/07
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Val: 1.68.1001C.10V

ALT: 22.10037.191

2010/04/07
10uH Choke
Val: 1.68.1001C.10V

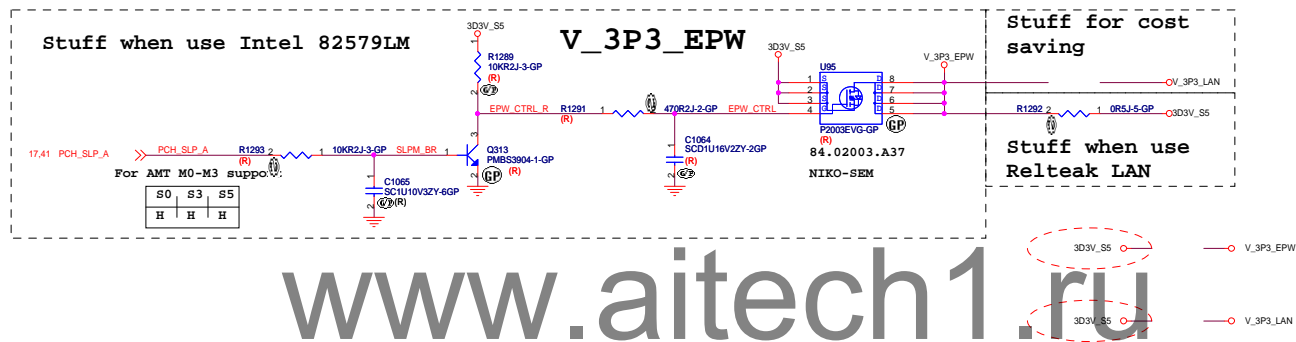
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2010/04/07
10uH Choke
Val: 1.68.1001C.10V

ALT: 22.10037.191

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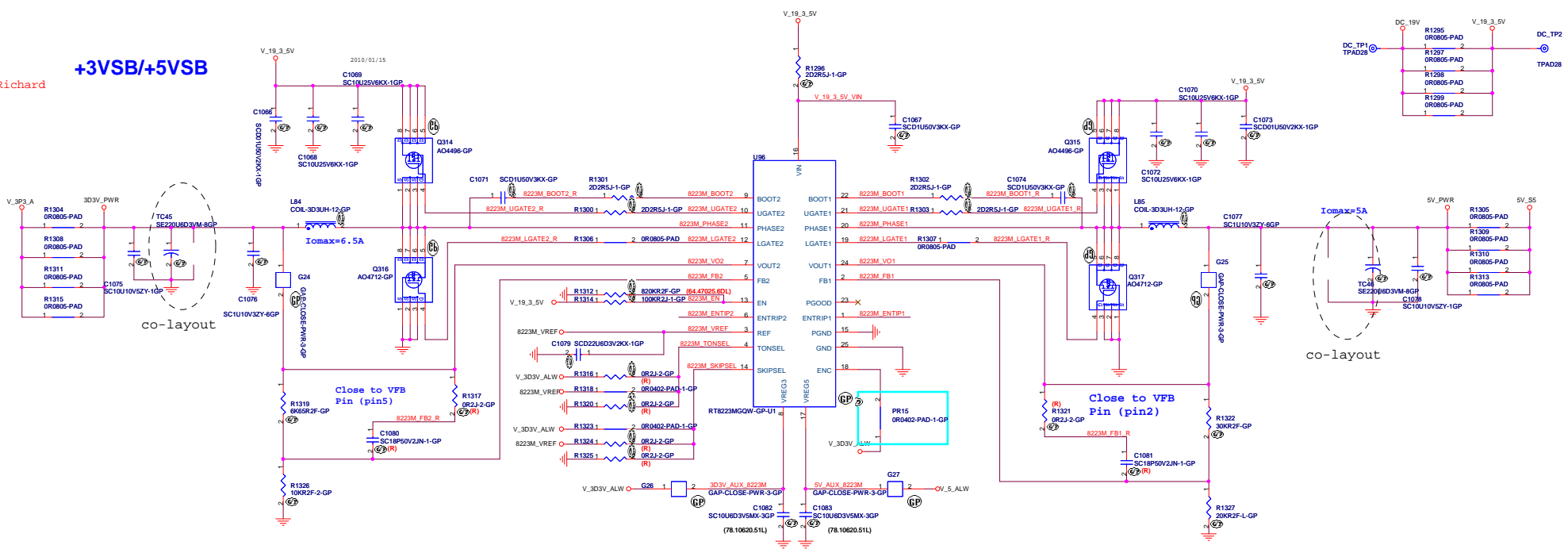
For Mini-PCIE



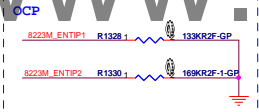
PC_PWRGD

2010.0823.Richard

+3VSB/+5VSB

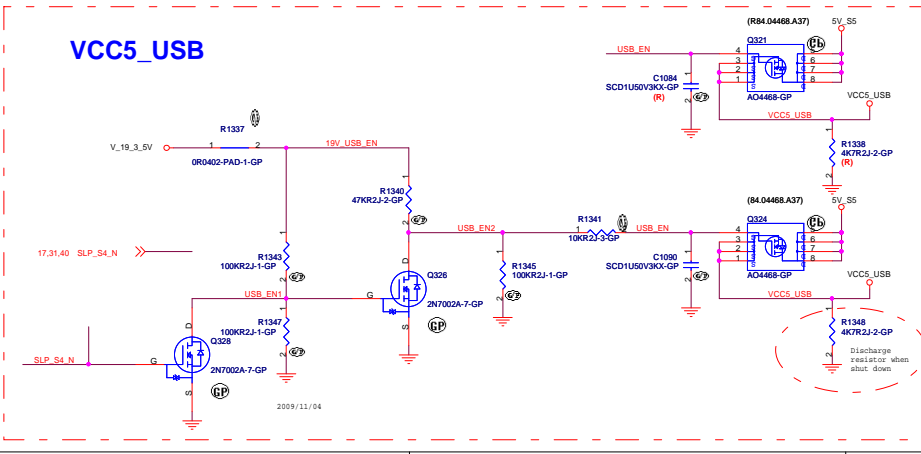
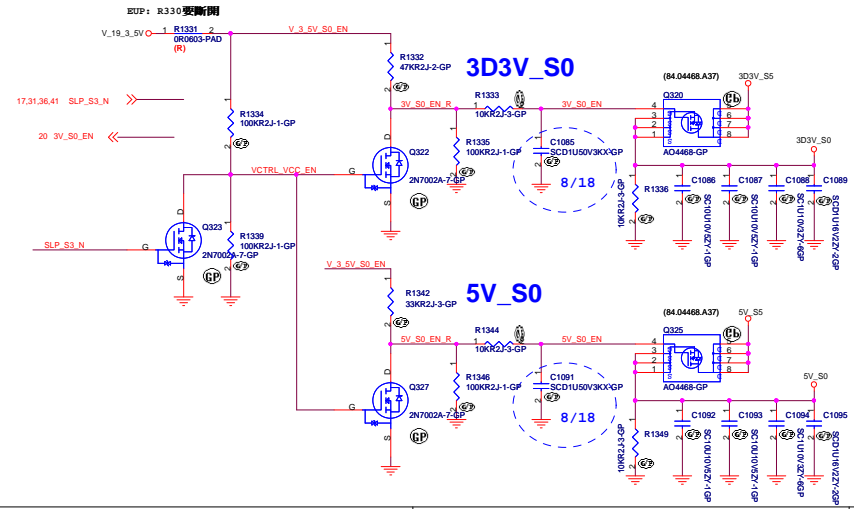


	GND	VREF	VREG3	VREG5
SKIPSEL	PWM	SKIP	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	330k/CH1 375k/CH2	400k/CH1 500k/CH2	400k/CH1 500k/CH2

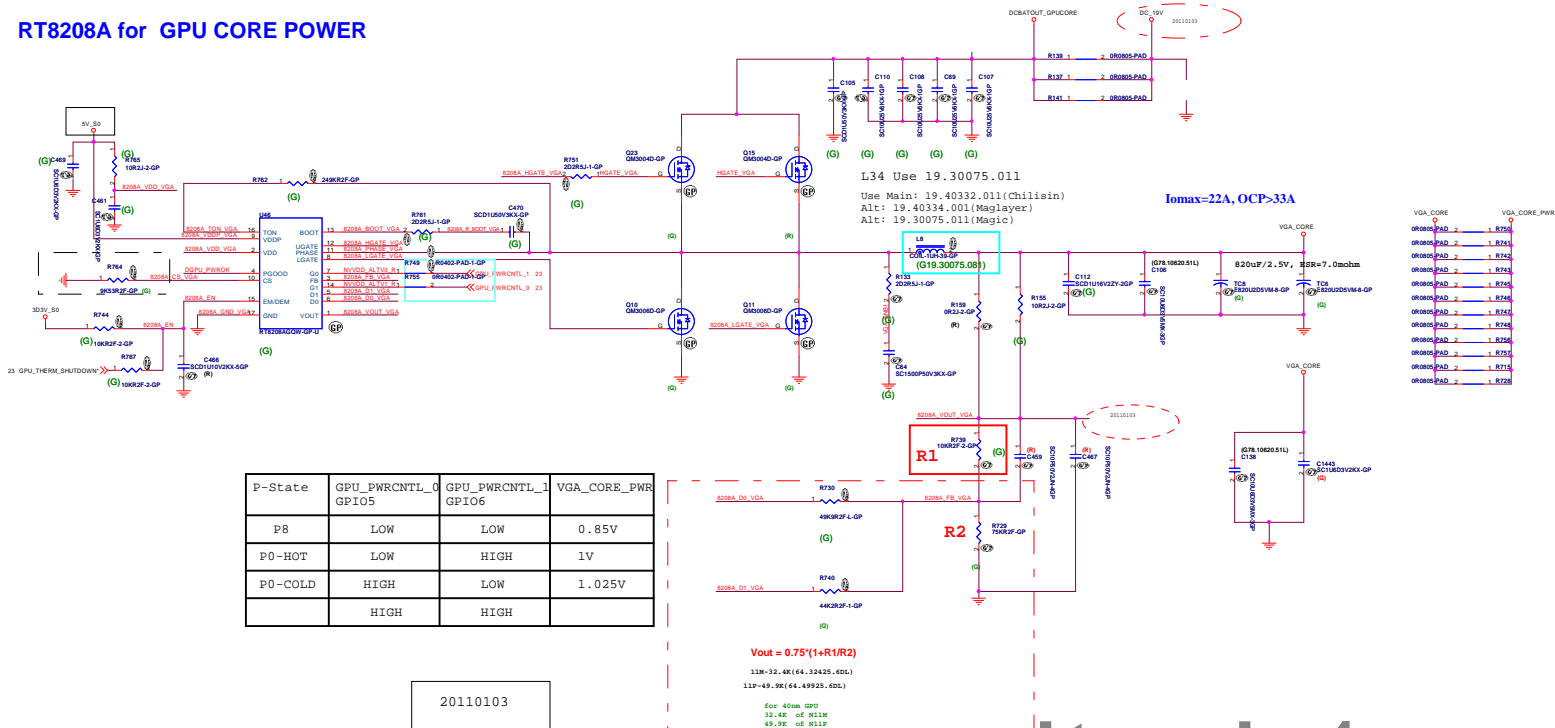


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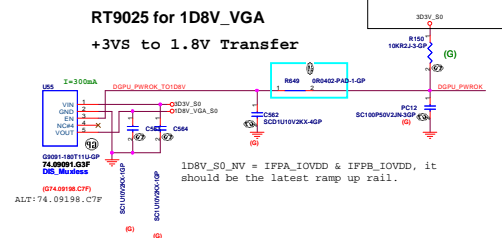
20100103



RT8208A for GPU CORE POWER

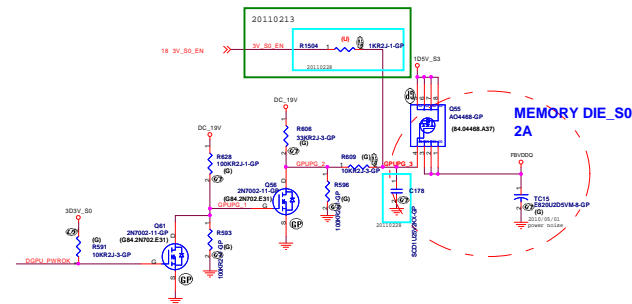


P-State	GPU_PWRCNTL_0 GPI05	GPU_PWRCNTL_1 GPI06	VGA_CORE_PWR
P8	LOW	LOW	0.85V
P0-HOT	LOW	HIGH	1V
P0-COLD	HIGH	LOW	1.025V
	HIGH	HIGH	




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```
20110103
GPU VCORE -> MEMORY POWER
```



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		Wistron Incorporated 12F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title			
CPU VSA			
Size	Document Number		Rev
C	Zappa		SA
Date:	Thursday, January 06, 2011	Sheet	43 of 52

VSA_PWRGD

10 VCC_SENSE

10 VSS_SENSE

10 H_VDSOUT_VR

10 H_VIDCK_VR

10 H_VIDALERT_VR

45 PWM1

45 CSN1

45 CSP1

45 PWM2

45 CSN2

45 CSP2

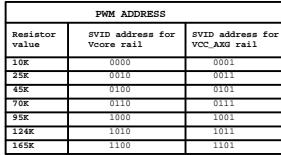
45 PWM3

45 CSN3

45 CSP3

CPU AXG POWER

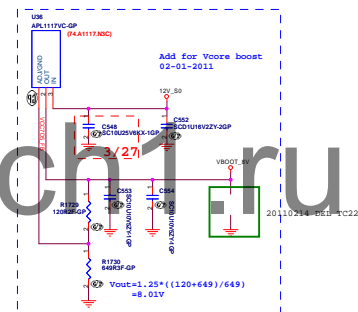
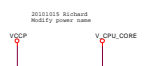
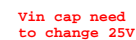
10,58 H_PROCHOT_N <<-




BOOT VOLTAGE	
Resistor value	Boot Voltage
10K	0V
25K	0.85V
45K	0.9V
70K	0.95V
95K	1V
124K	1.1V
165K	1.5V

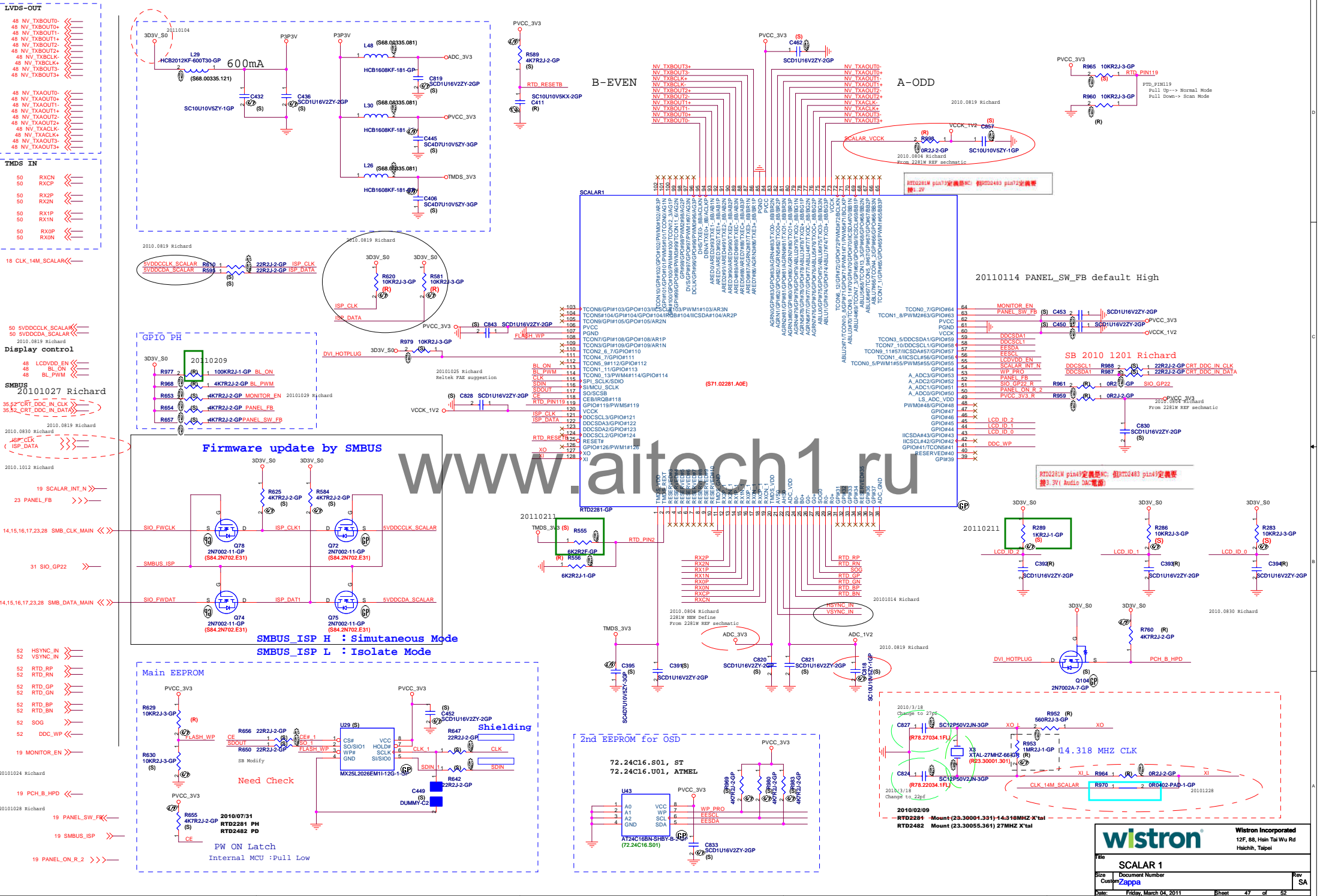
Vin cap need
to change 25V

84.04809.036	NTD4809	84.04806.036	NTD4806
Vgs @ 4.5V,		Vgs @ 4.5V,	
Id = 45A,		Id = 59A,	
Rds(on) = 12-14mohm,		Rds(on) = 7.9-9.4mohm	
Qg = 11-13nC		Qg = 15-23nC	



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		Wistron Incorporated 12F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title			
Size B	Document Number Zappa		Rev SA
Date:	Sunday, January 02, 2011		Sheet 46 of 52



LVDS@GPU

23 MCU_PANEL_ON >>>—

Low: Disable

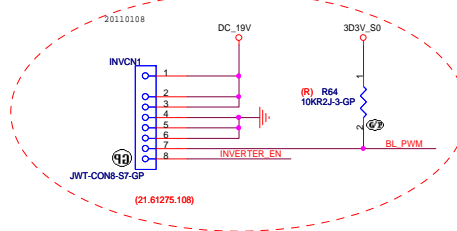
DEL Printer Port

DEL Printer Port

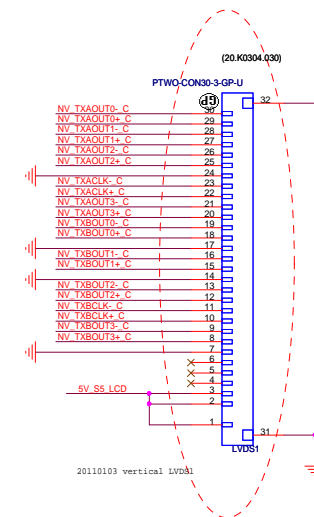
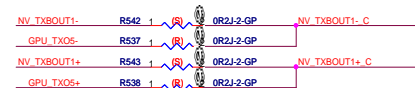
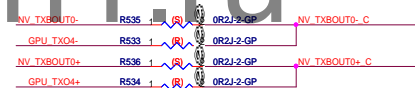
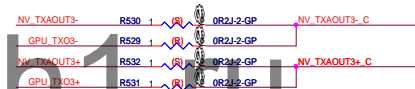
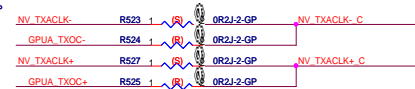
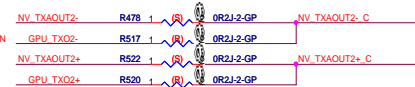
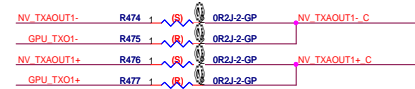
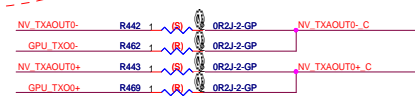
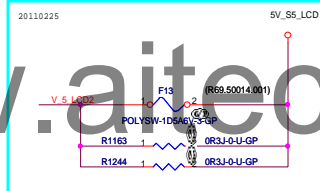
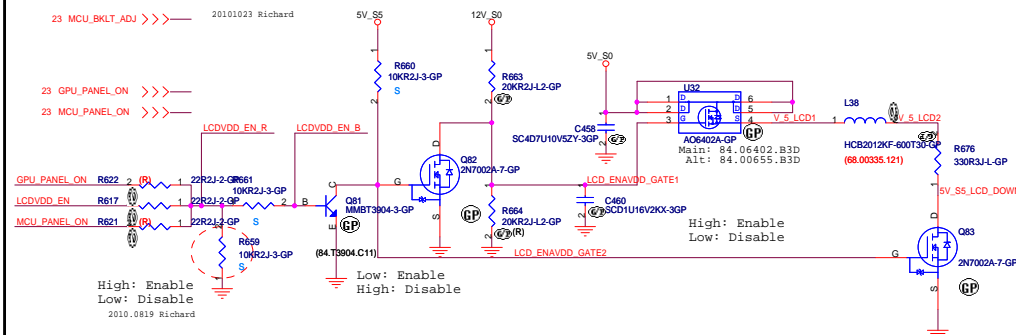
```
Use OD type
High: SMBUS to VGA DDC
Low : disable (default)
```

```
Scalar
```

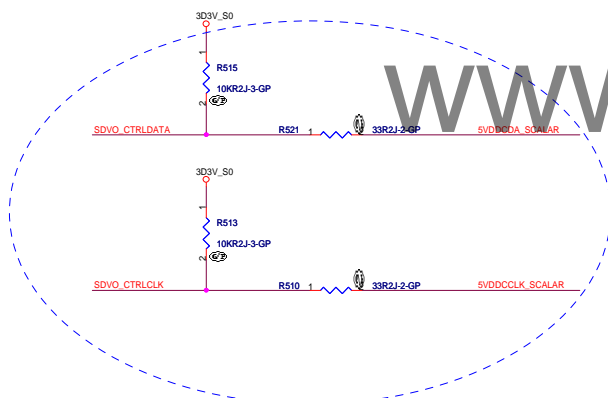
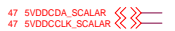
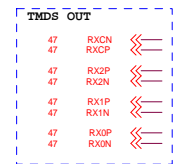
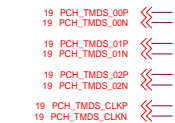
	<< SVDCCCLK_SCALAR	47.50
	<< SVDCCDA_SCALAR	47.50



INVERTER BOARD CONNECTOR

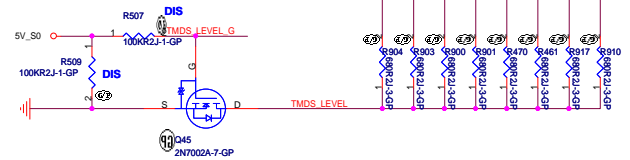


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DIGITAL SIGNAL IN



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<Variant Name>		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title RUN POWER			
Size C	Document Number Zappa		Rev SA
Date:	Sunday, January 02, 2011	Sheet	51 of 52

VGA IN

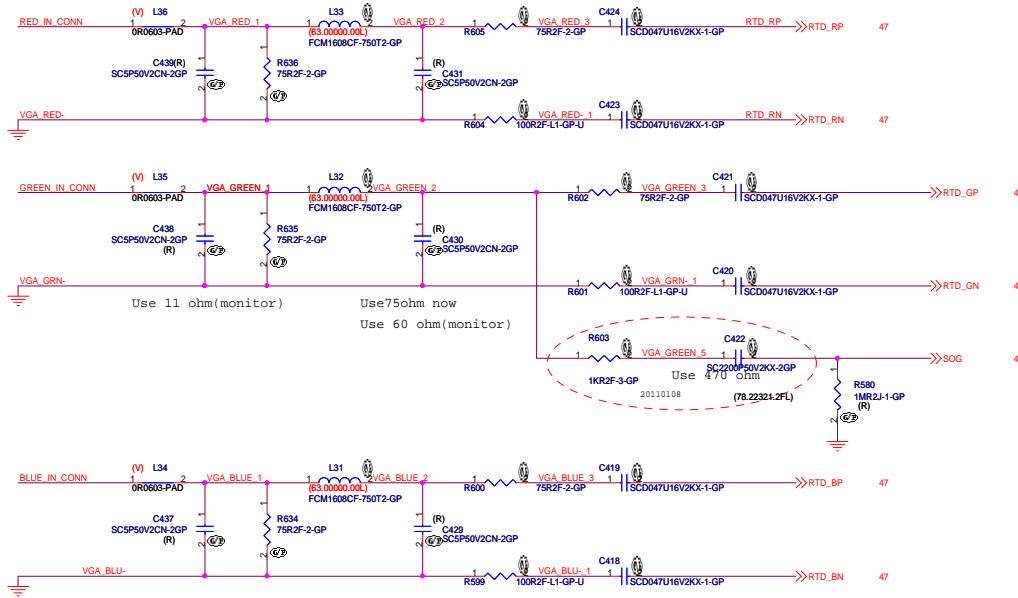
35 RED_IN_CONN
35 GREEN_IN_CONN
35 BLUE_IN_CONN
35 HSYNC_IN_CON
35 VSYNC_IN_CON
35,47 CRT_DDC_IN_CLK
35,47 CRT_DDC_IN_DATA

VGA To Scalar

47 RTD_RP
47 RTD_RN
47 RTD_GP
47 RTD_GN
47 RTD_BP
47 RTD_BN
47 SOG
47 DDC_WP
47 HSYNC_IN
47 VSYNC_IN

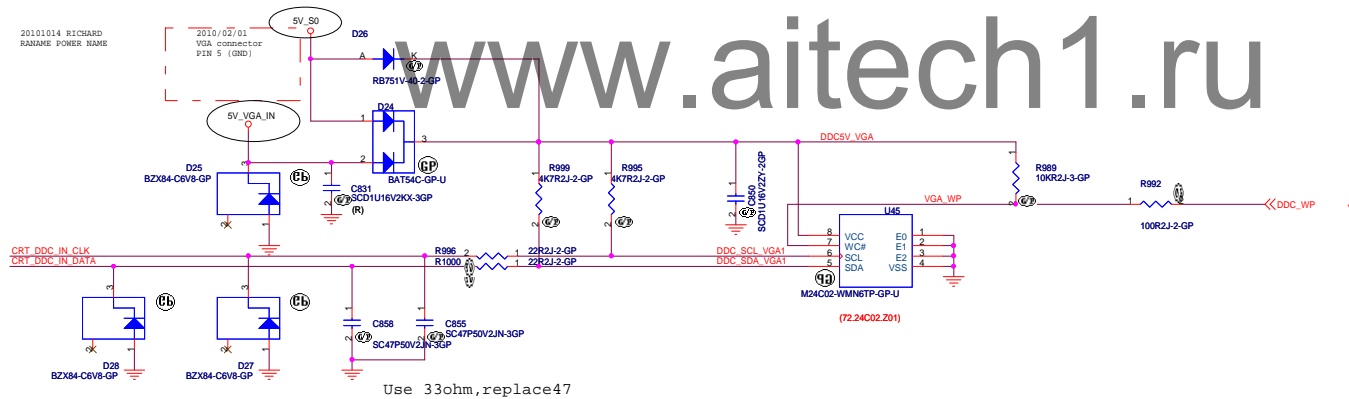
RGB

LPF place near Scalar

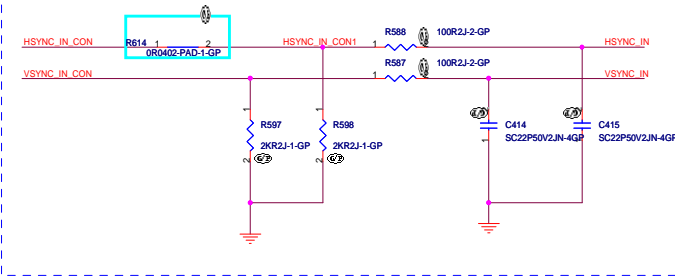


EDID

20101014 RICHARD
BANNAME POWER NAME



SYNC



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